赛灵思 **All** Programmable **SoC**技术及应用

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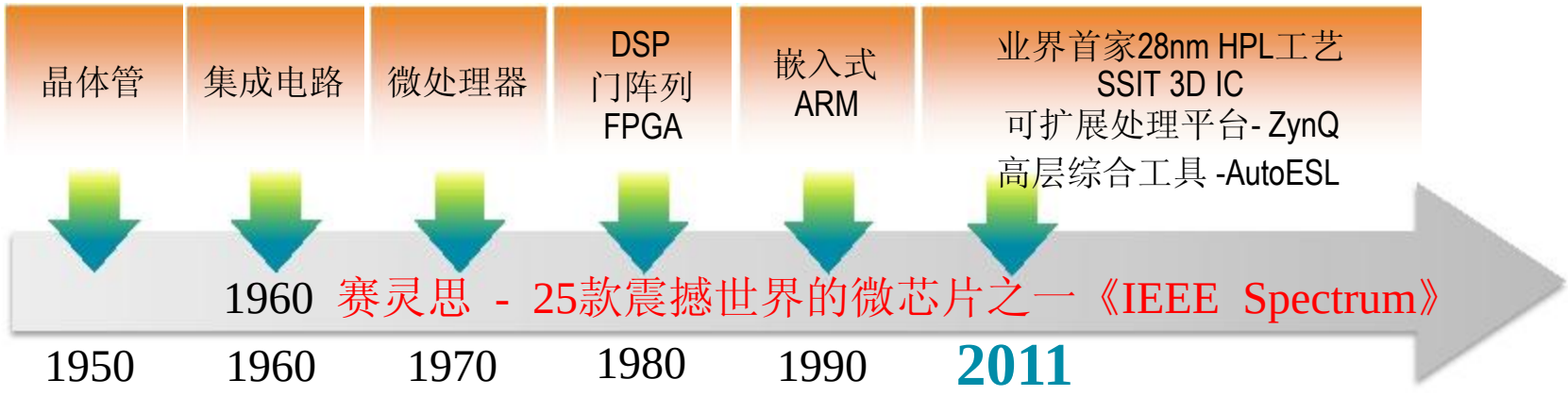
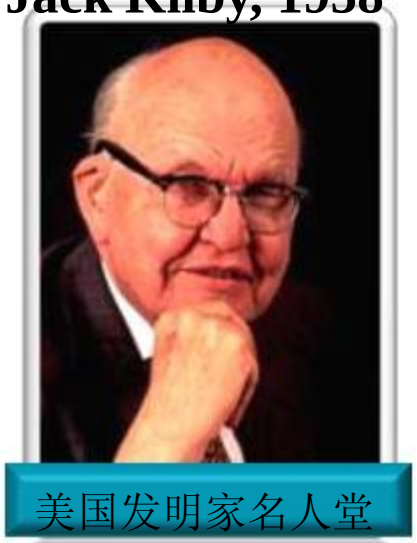
赛灵思 –创新是我们的DNA

赛灵思的技术创新得到业界认可

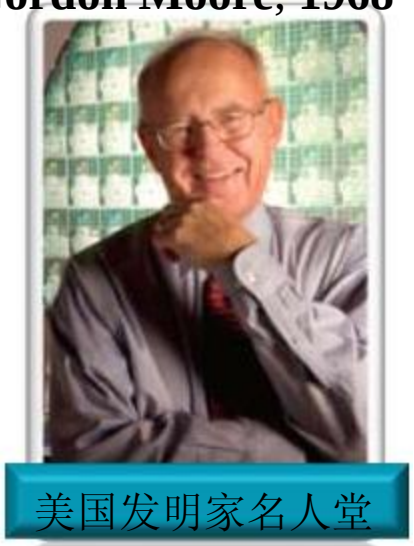


集成电路的发明者
Jack Kilby, 1958



美国发明家名人堂

摩尔定律的提出者
Gordon Moore, 1968



美国发明家名人堂

FPGA的发明者
Ross Freeman, 1984

美国发明家名人堂

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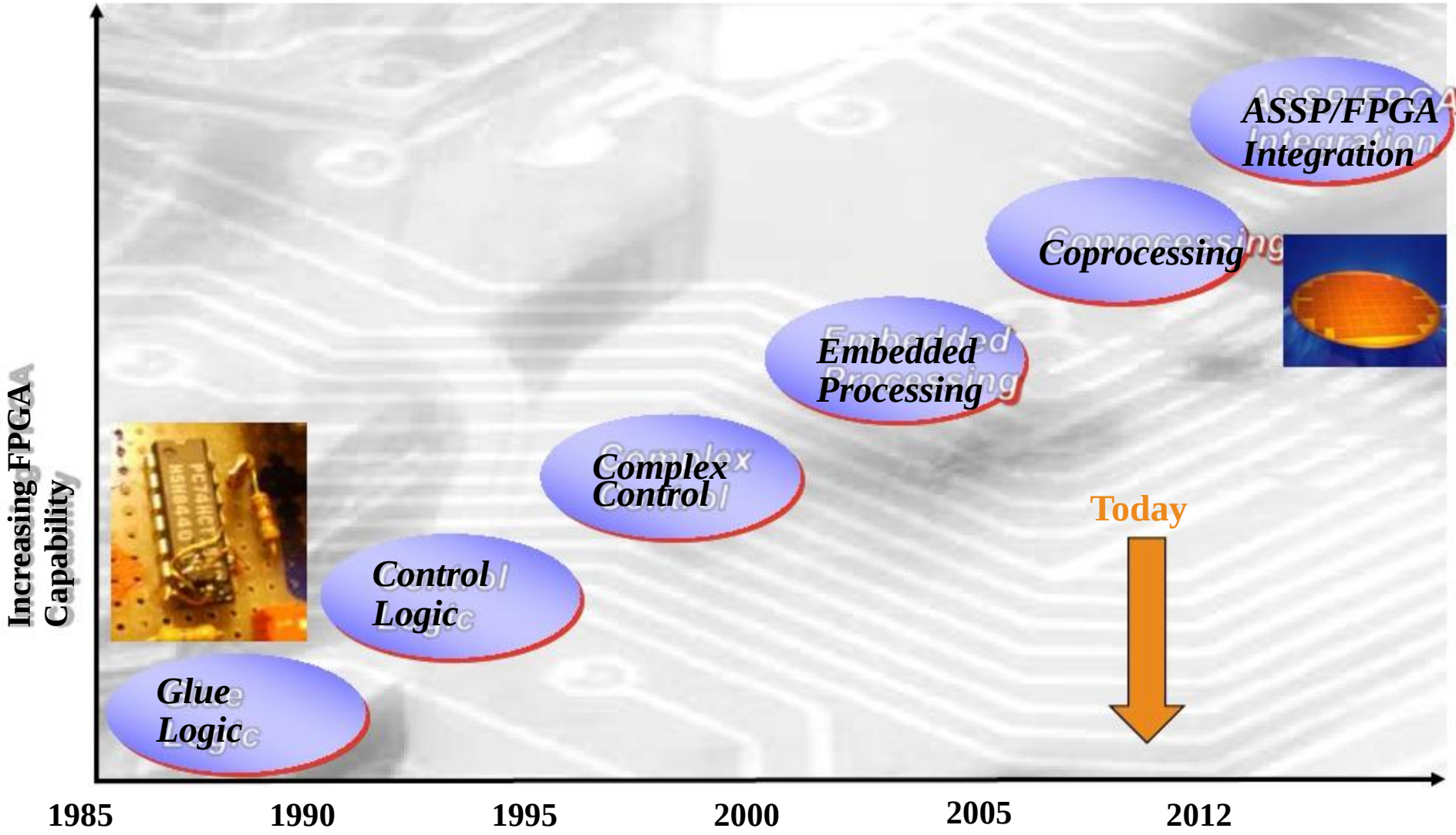
FPGA的持续演进



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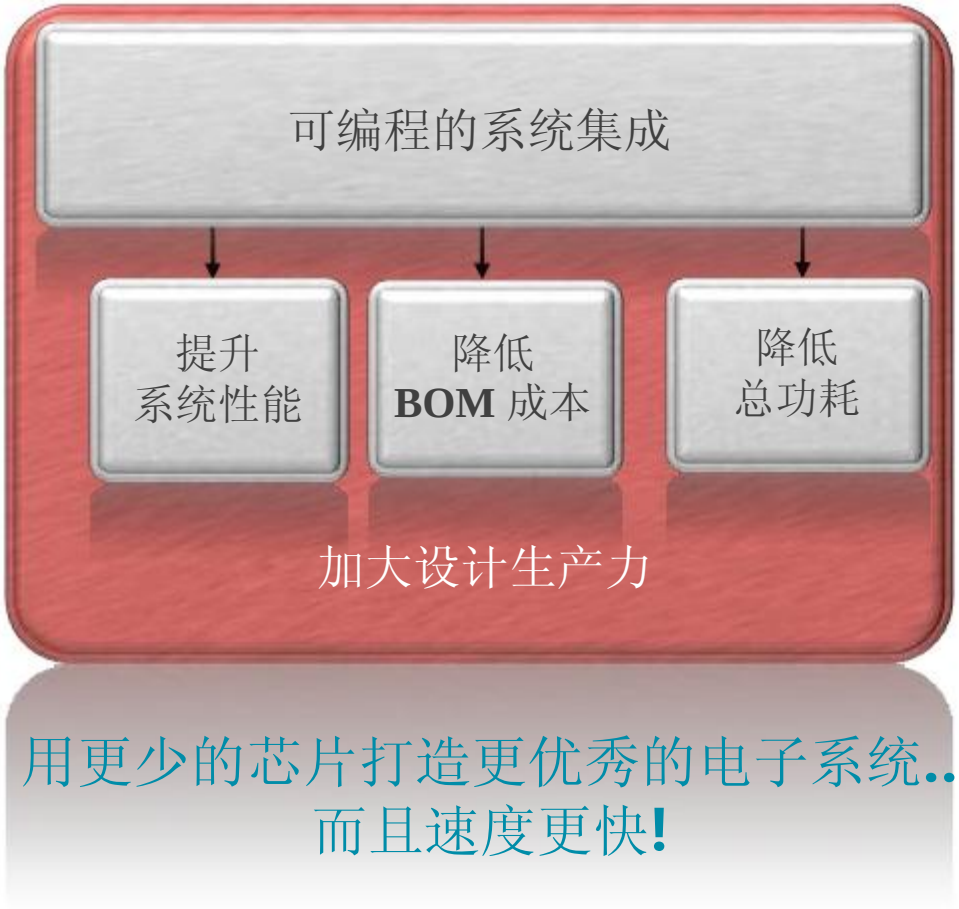
为什么 All Programmable?



用更少的芯片打造更优秀的电子系统....
而且速度更快!

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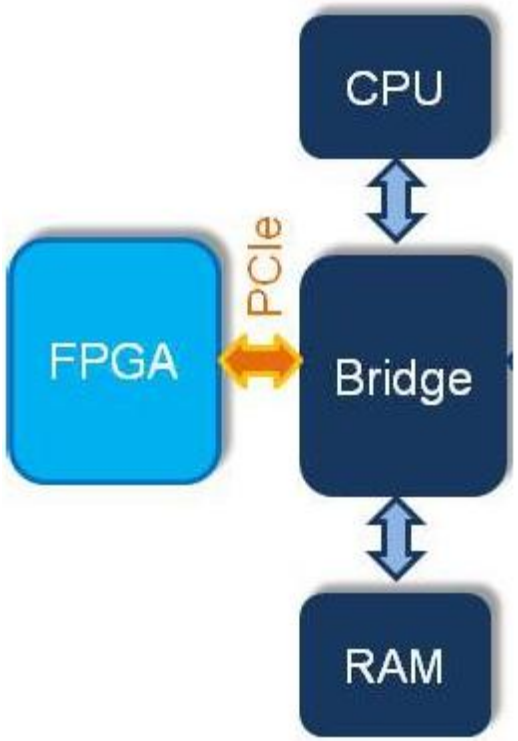
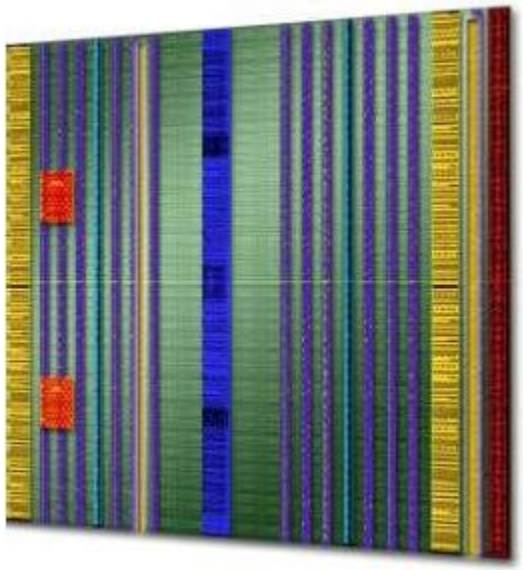
All Programmable SoC是系统集成的创新

- 分离方案



- 集成方案



"A symbiosis of CPU and FPGA on one die to reduce cost and PCB space!"

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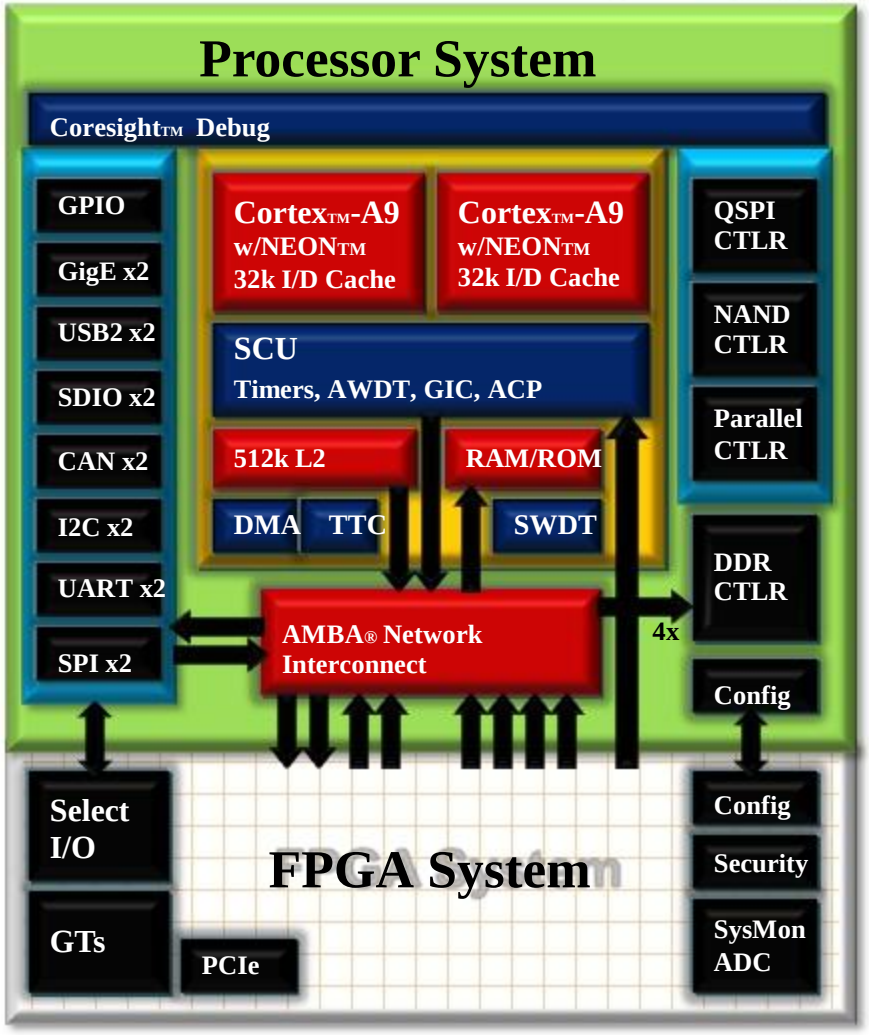
全球首家 All Programmable SoC
*ZynQ-7000*系列

EETimes/EDN
2012 ACE SoC of the Year

软件可编程
硬件可编程



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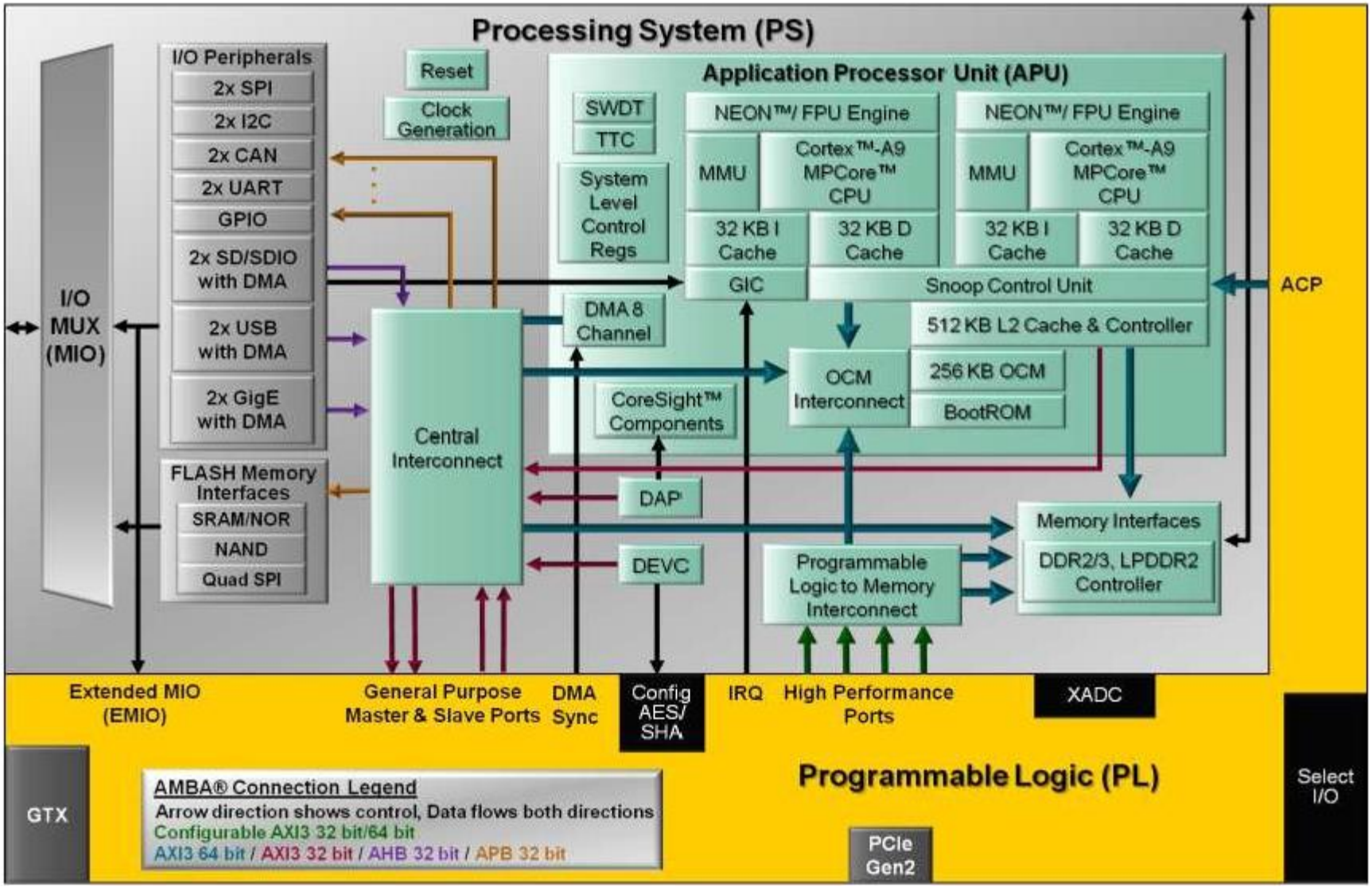
Zynq All Programmable SoC
系统框图



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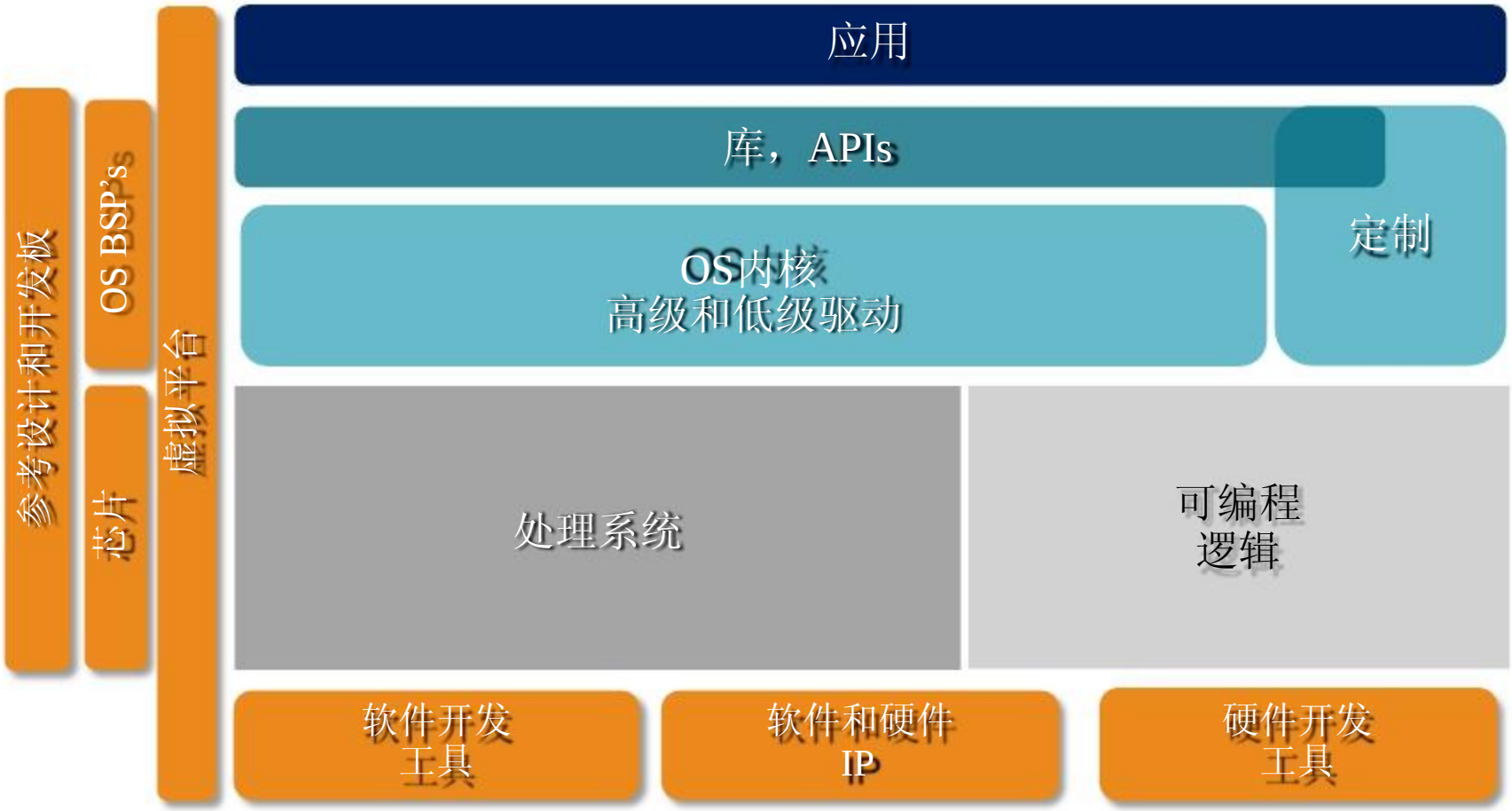
All Programmable SoC开发平台



提供的不仅仅是芯片 – 而是一个完整的开发平台

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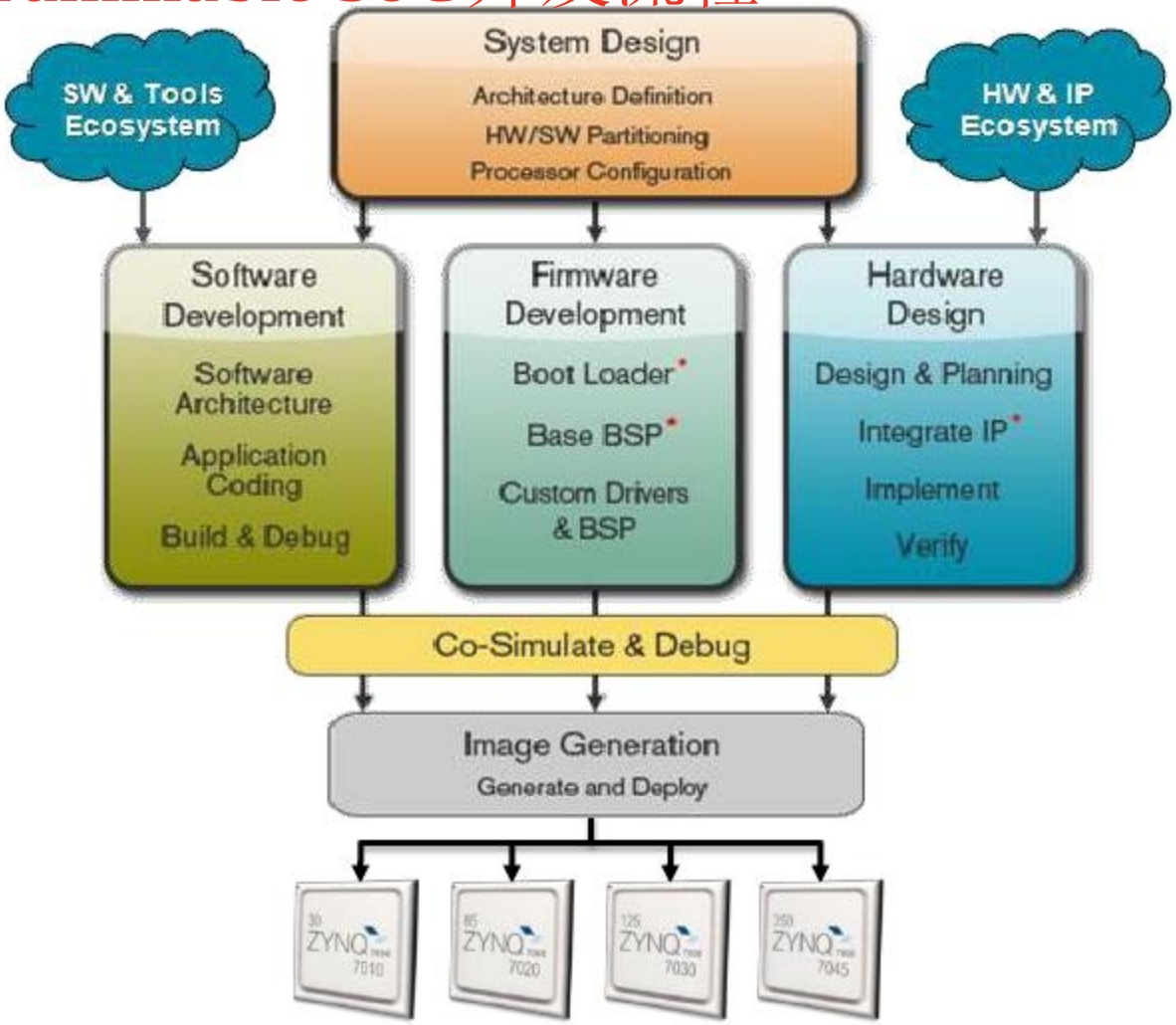
All Programmable SoC开发流程



用于开发**Zynq-7000 EPP**解决方案的丰富工具

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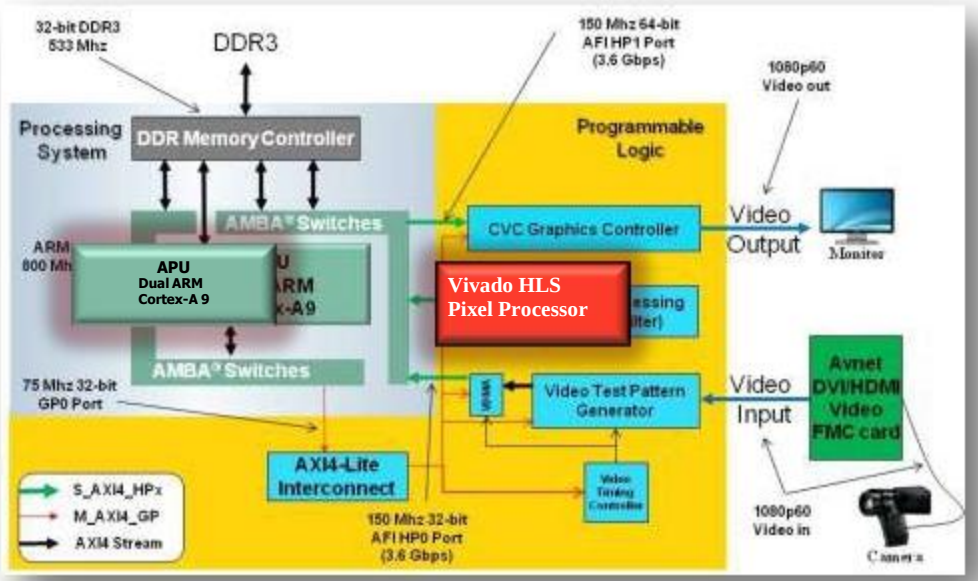
Vivado HLS加速All Programmable SoC设计

- **Customers can write and validate in C**
  - Easily Faster than any RTL simulator
  - Development does not get any more productive than C
- **Design Exploration**
  - Don’t just create a design: you have the time to create the right design
- **Easily Integrate**
  - Seamless IP integration with Xilinx tools
- **Enabling Programmable Systems**
  - Execute the algorithm on the CPU
  - Execute the algorithm in the FPGA fabric
  - We are ALL PROGRAMABLE

ZC702 System Overview



Implement C algorithm in FPGA Fabric

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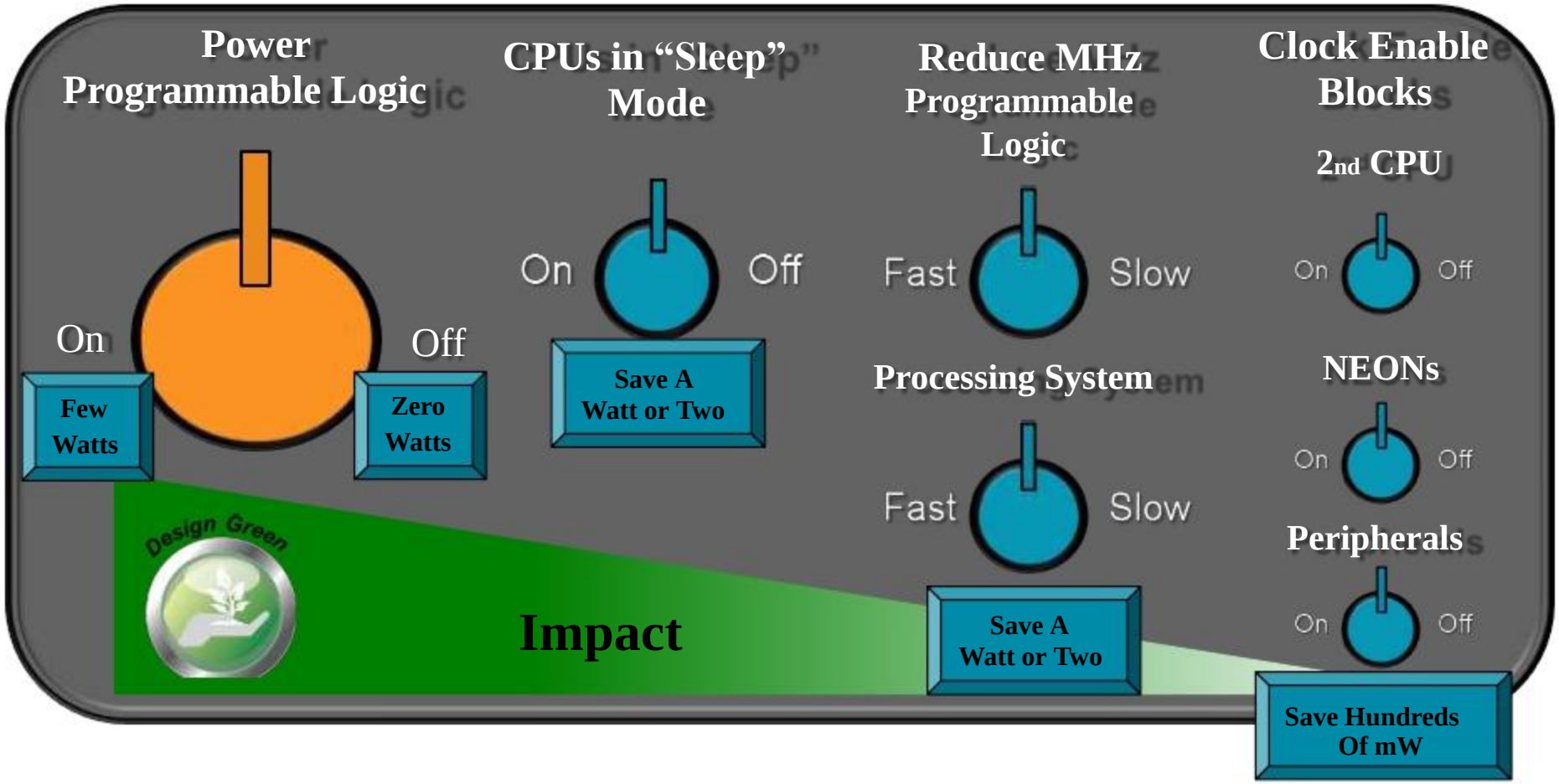
All Programmable SoC的功耗管理



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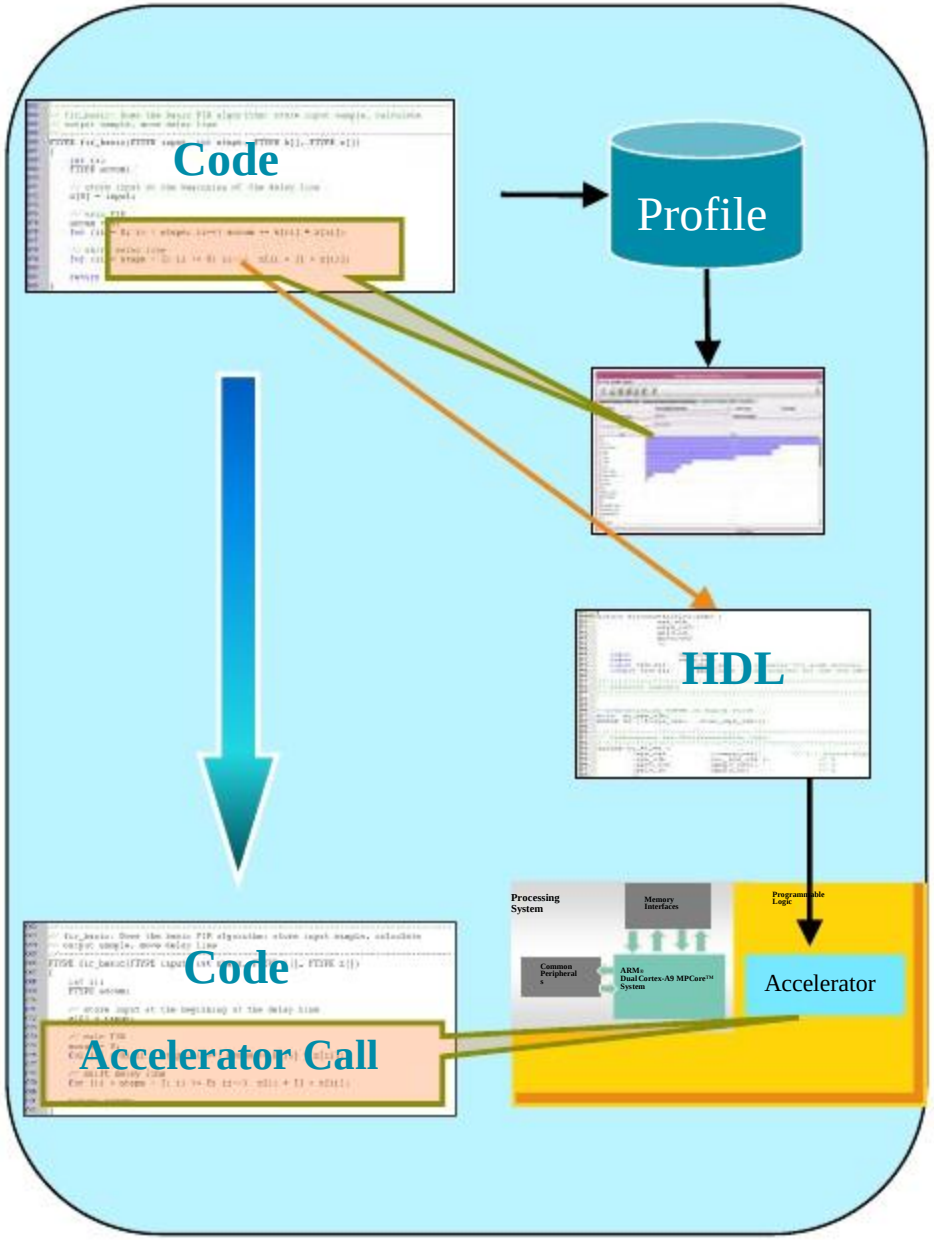
如何创建硬件加速器

- Create Code
- Profile Code
- Identify Critical Code Segments
- Translate Critical Code to HDL
- Build HW Accelerators from HDL
- Replace Critical Code with Calls to HW Accelerators

- Potential code acceleration of 10+ times



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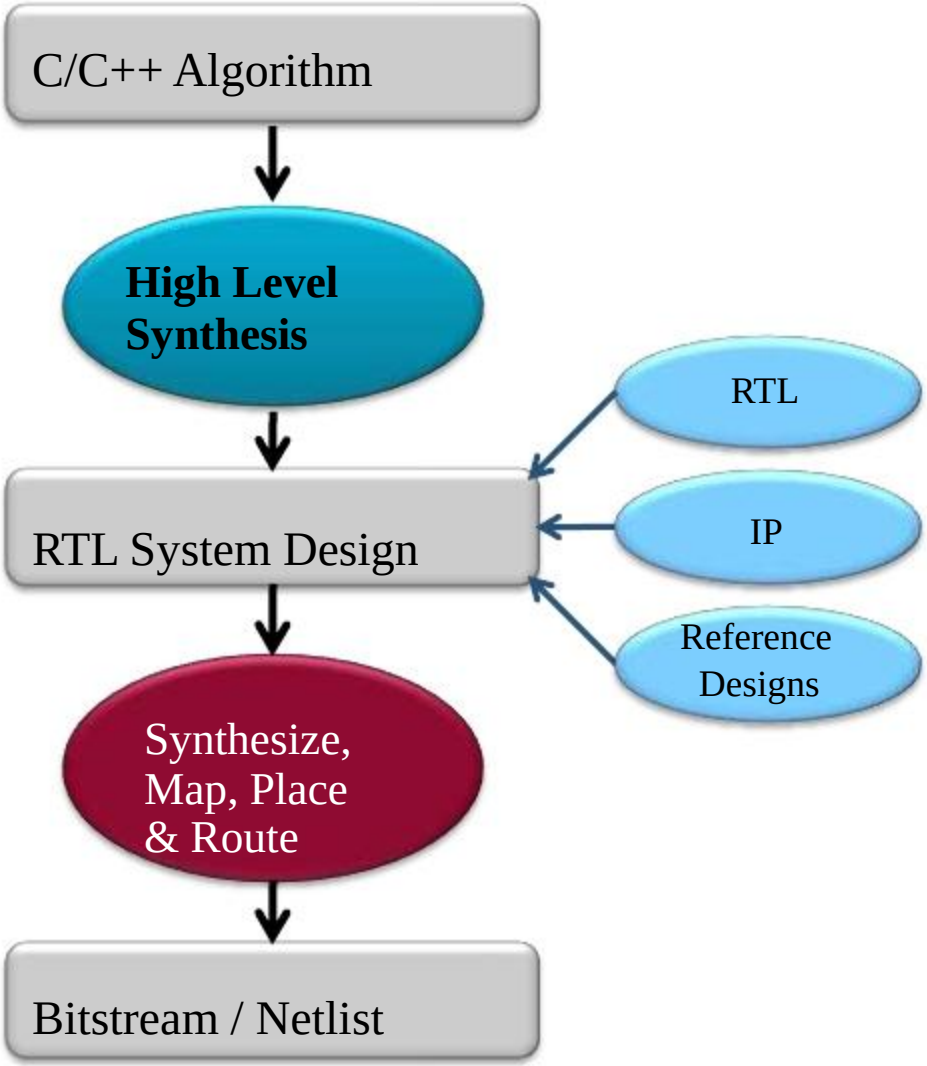
HLS流程

- **Enables embedded programmers to target FPGAs**
- **Delivers Productivity Increase for RTL Designers**
  - **Create multiple solutions**
  - **Design verification**



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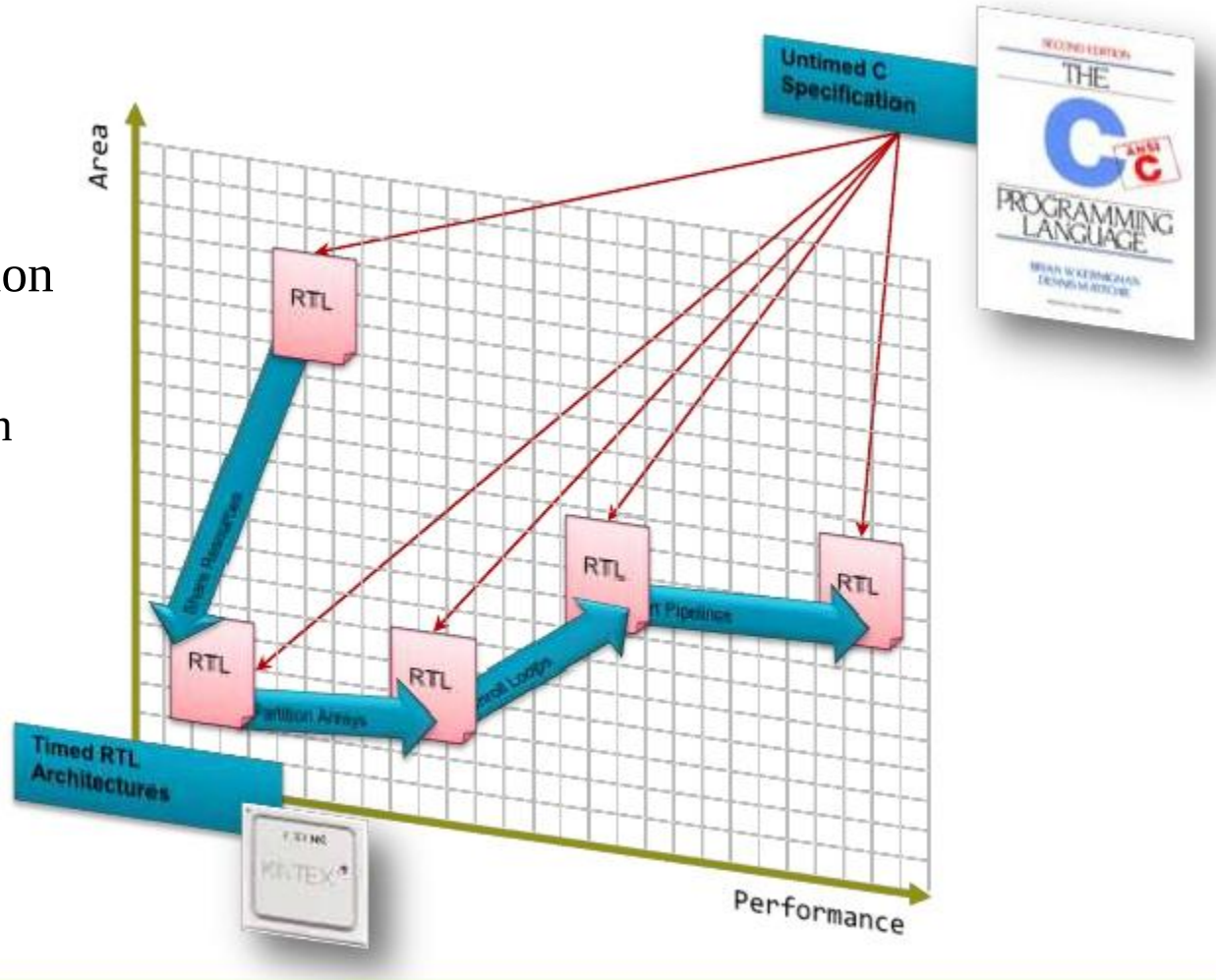
XILINX ALL PROGRAMMABLE.

HLS使架构探索更容易

- **Permutability**
  - Architecture Exploration
    - Timing
      - Parallelization
      - Pipelining
    - Resources
      - Sharing
  - Better QoR



Rapid design exploration delivers QoR rivaling hand-coded RTL

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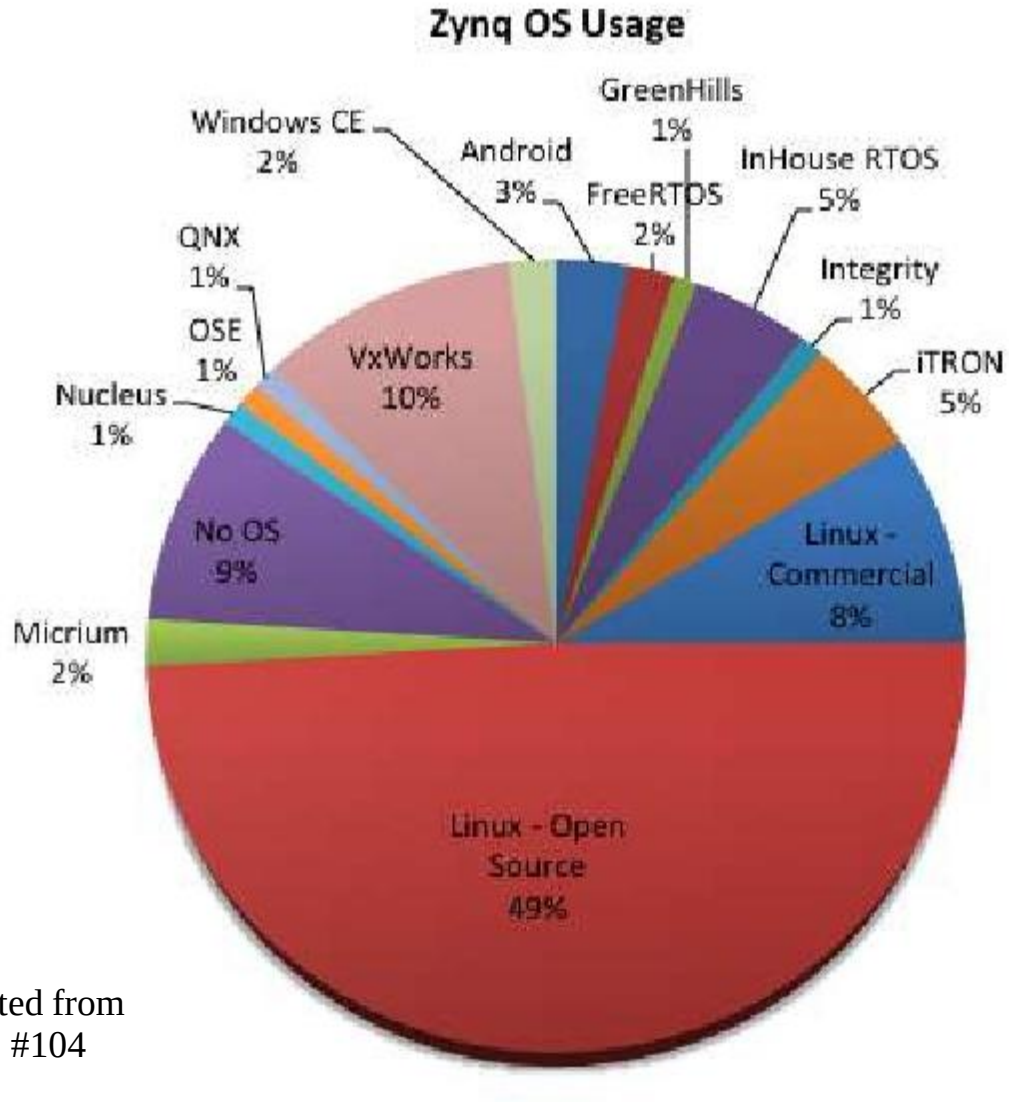
All Programmble SoC的操作系统支持



* Based on data collected from early access customers #104

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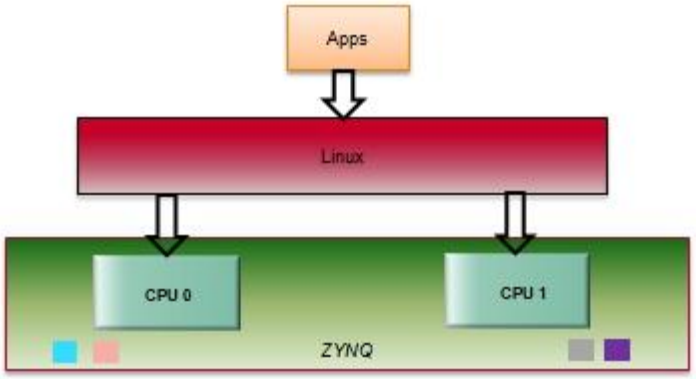
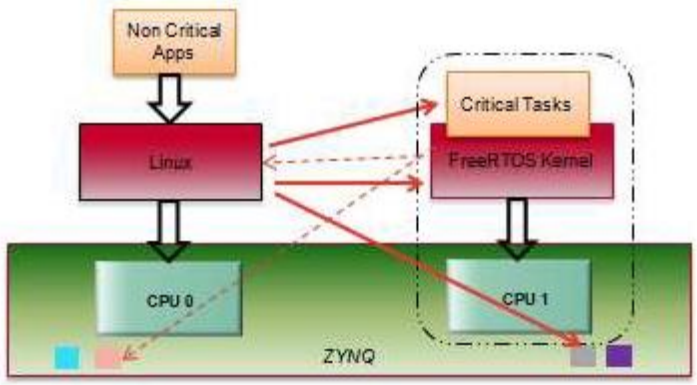
All Programmable SoC的OS配置

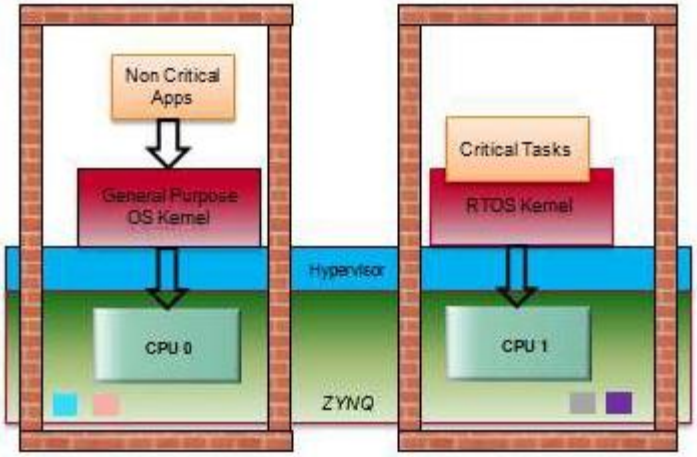
SMP



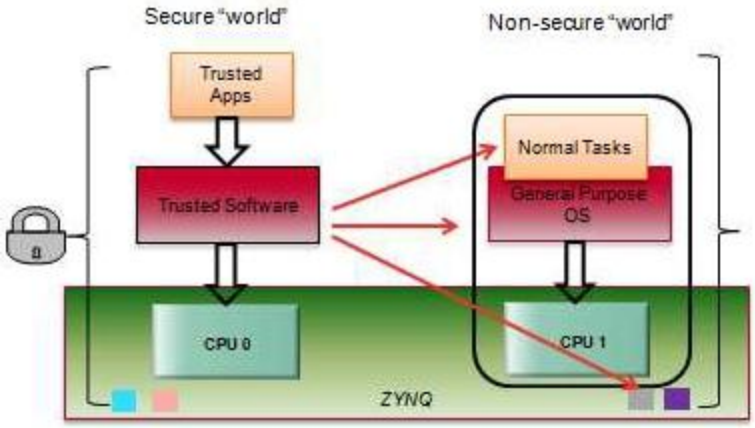
AMP



Hypervisor



Trustzone



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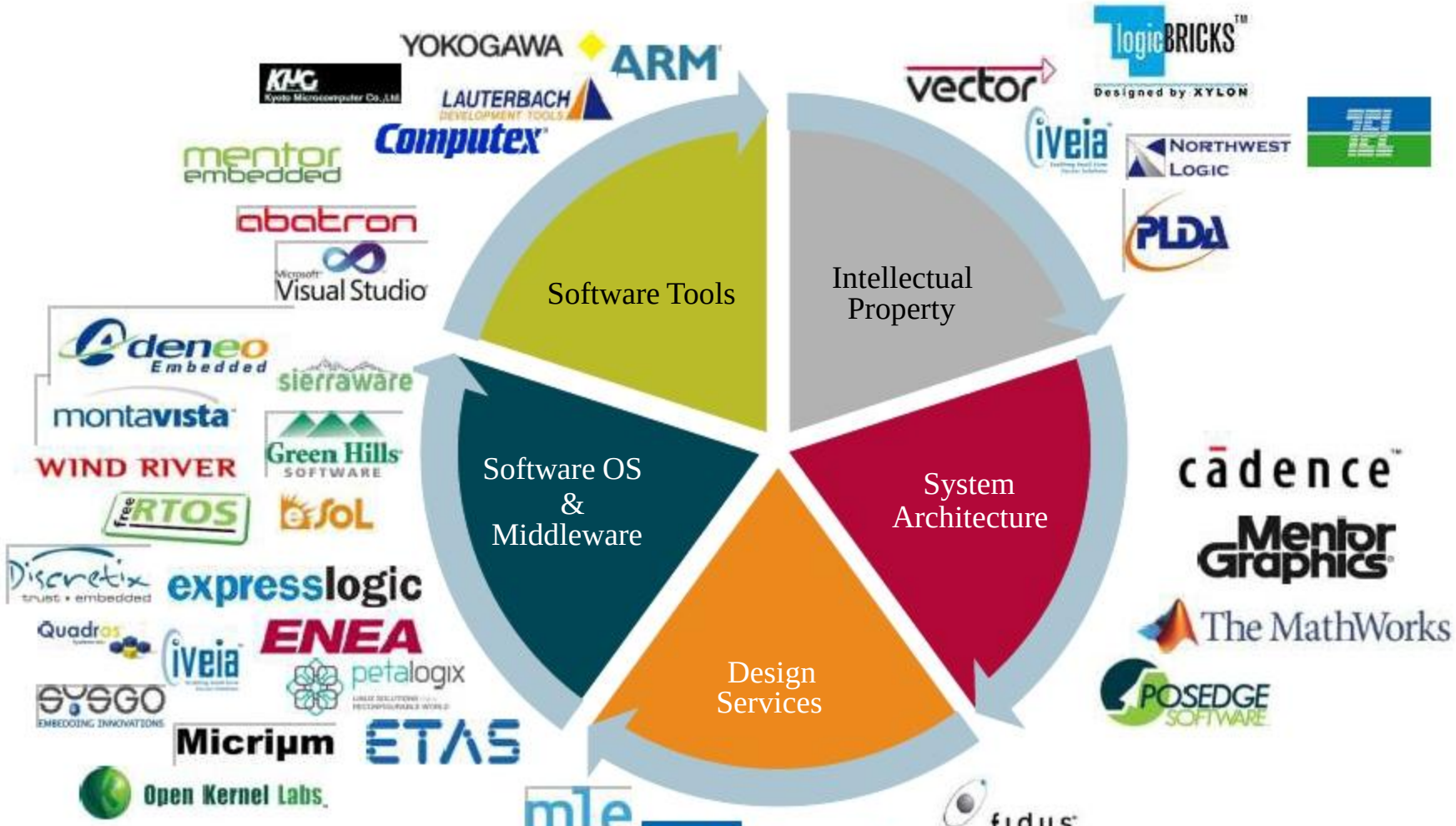
All Programmable SoC生态系统



. . . as of September 2012

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All Programmable SoC开发资源

ZC702/706

Zedboard

Zingboard

Zedboard community

Zynq wiki page

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All Programmable SoC的广泛应用

有线通信
- 互联网

无线通信
- 3G到4G的演进

消费电子产品
- 3D电视

广播电视
- 3D摄像机

工业
- 智能电网

测试，测量
- 新业务测试仪

汽车电子
- 车载娱乐系统
- 安全系统

安防监控
- 联网视频监控

医疗电子
- 超声设备

计算及数据存储
新药品研究

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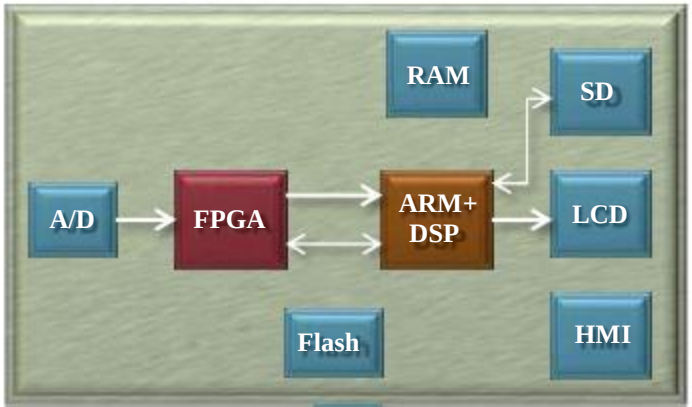
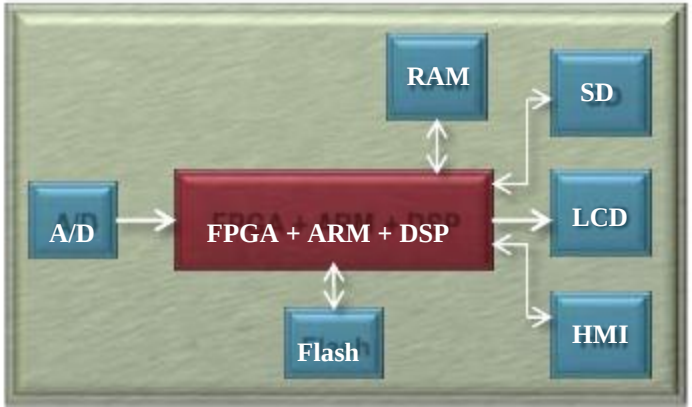
Zynq 医疗便携超声设备

Today's Solution



Zynq Solution



Integration
2 or 3 Chips → 1 Chip

Perf.	Cost	Power
+ 2X	- 40%	- 50%

Productivity
> 50%

Matlab, AutoESL, IP Reuse

2015 Medical SAM: $400M

Source: Xilinx Estimates

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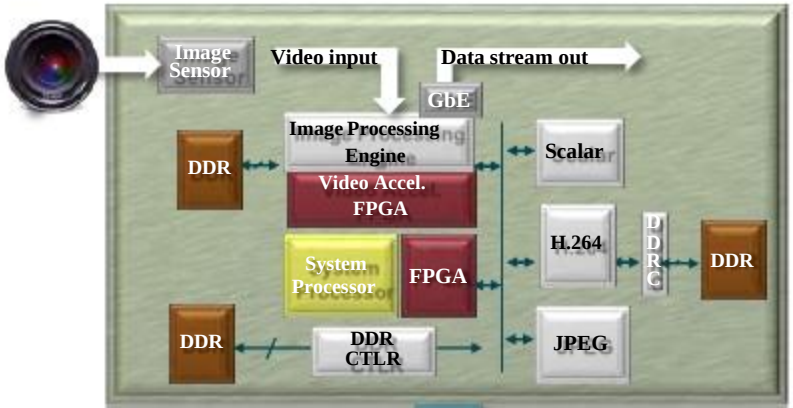
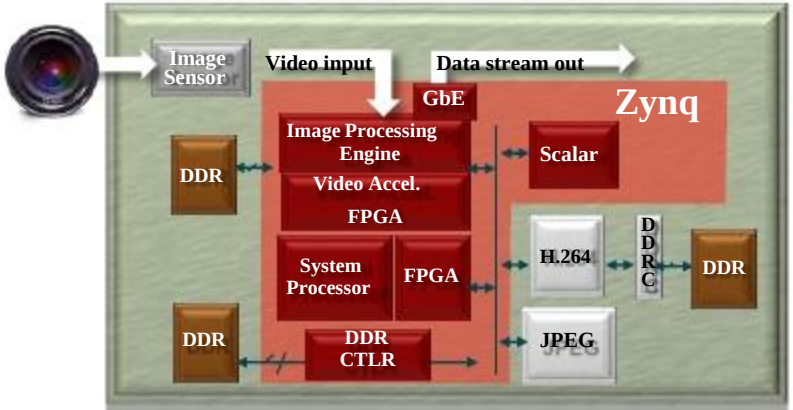
Zynq 智能监控

Today's Solution



Zynq Solution



Integration
4 Chips → 1 Chip

Perf.	Cost	Power
+ 30%	- 50%	- 50%

Productivity
> 50%

AutoESL, IP Reuse

2015 Surveillance SAM: $350M

Source: Xilinx Estimates

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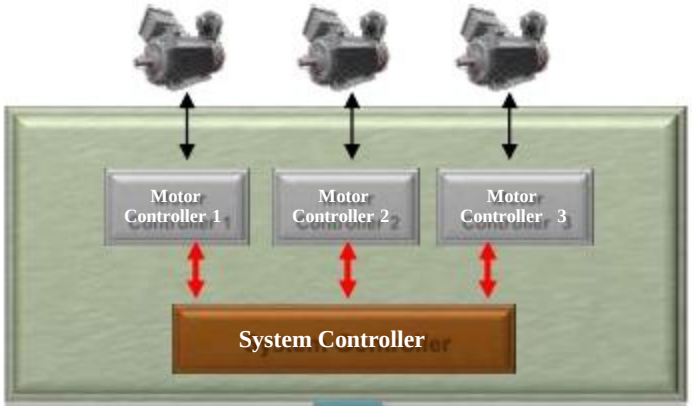
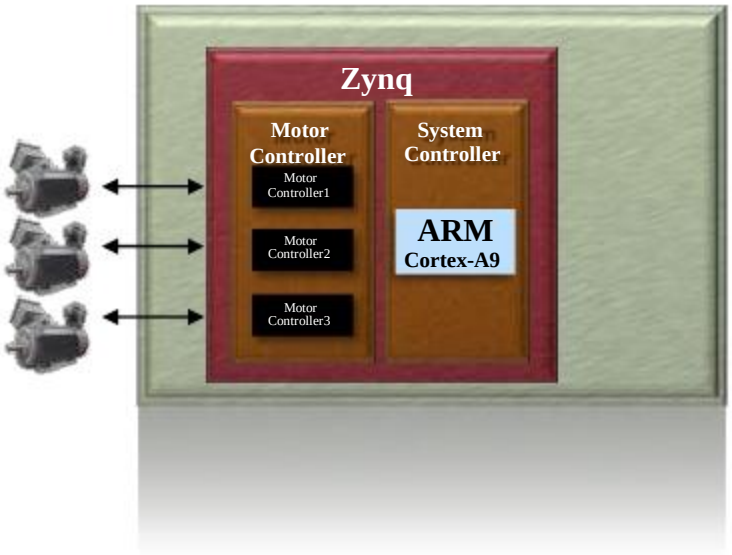
Zynq 马达控制

Existing Infrastructure



Zynq Solution



Integration
4 Chips → 1 Chip

Perf.	Cost	Power
+ 30%	- 20%	- 30%

Productivity
> 30%

TDP + IP Reuse

2015 Motor Control SAM: $260M

Source: Xilinx Estimates

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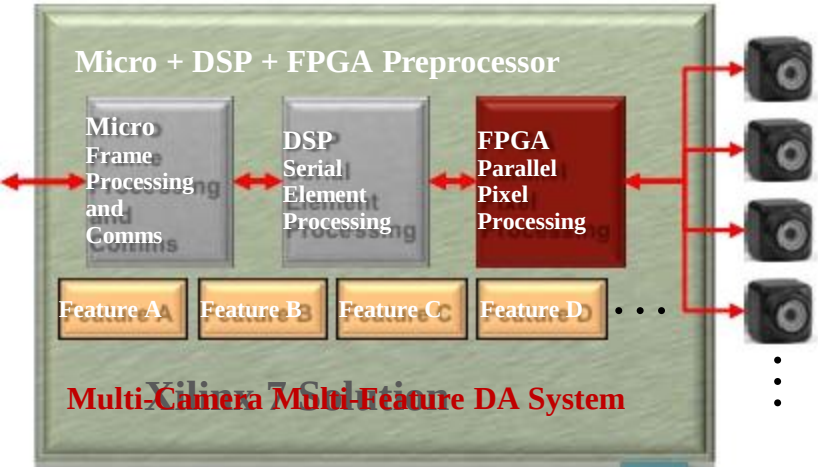
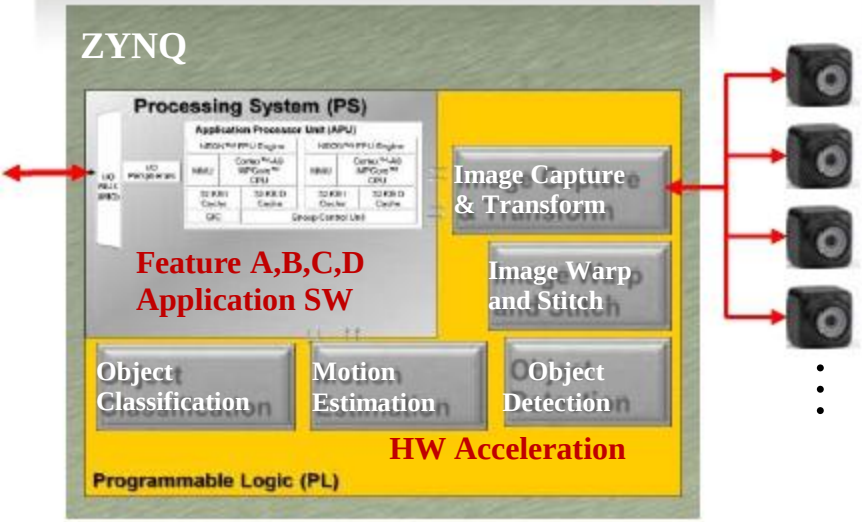
基于Zynq的汽车辅助驾驶

Existing Infrastructure



Zynq Solution



Source: Xilinx Estimates

Programmable Systems Integration

3 Chips → 1 Chip

System Perf	BOM Cost	Total Power
>130%	- 25%	- 50%

TDP Kit = Vehicle Demo in Weeks

Accelerated Design Productivity

- Example DA Features
  - Blind Spot Detection
  - 360 Degree Surround View
  - Lane Departure Warning
  - Pedestrian Detection

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总结

- 全力推动**All Programmable** 技术…既包括系统，也包括技术
- 全球首款**All Programmable SoC** 改变嵌入式市场格局
- **All Programmable SoC**推动中国“智”造

ALL PROGRAMMABLE SoC

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携手赛灵思

开创嵌入式设计**All** Programmable SoC 时代

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