京微雅格
Capital Microelectronics

嵌入式系统联谊会
www.esbf.org.cn

FPGA发展的昨天、今天和明天

副总裁：王海力博士

2015年12月

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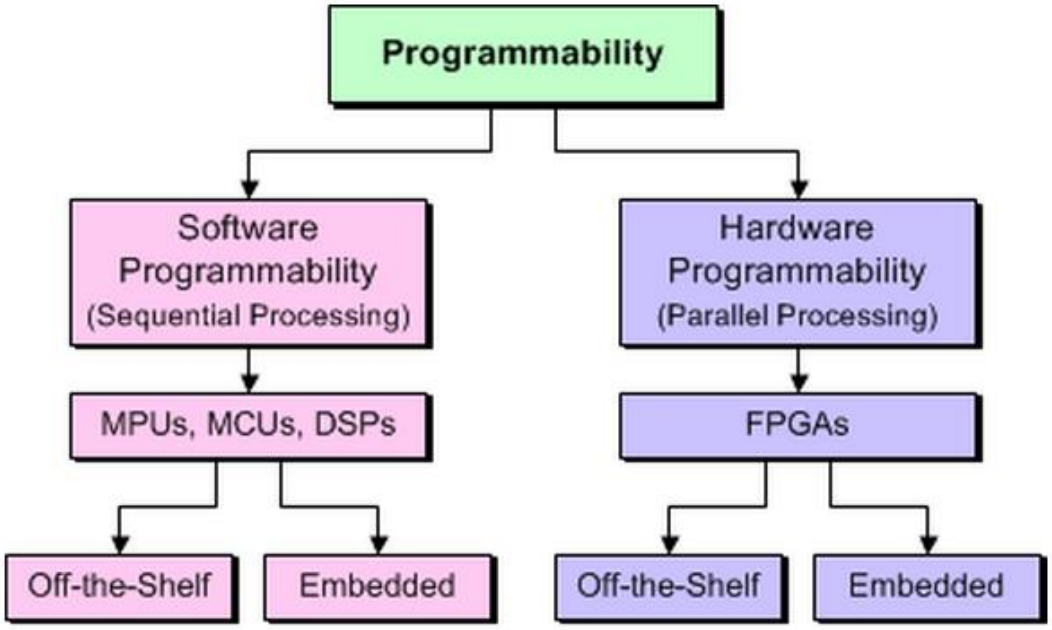
- 重温过去
- 思考现在
- 展望未来

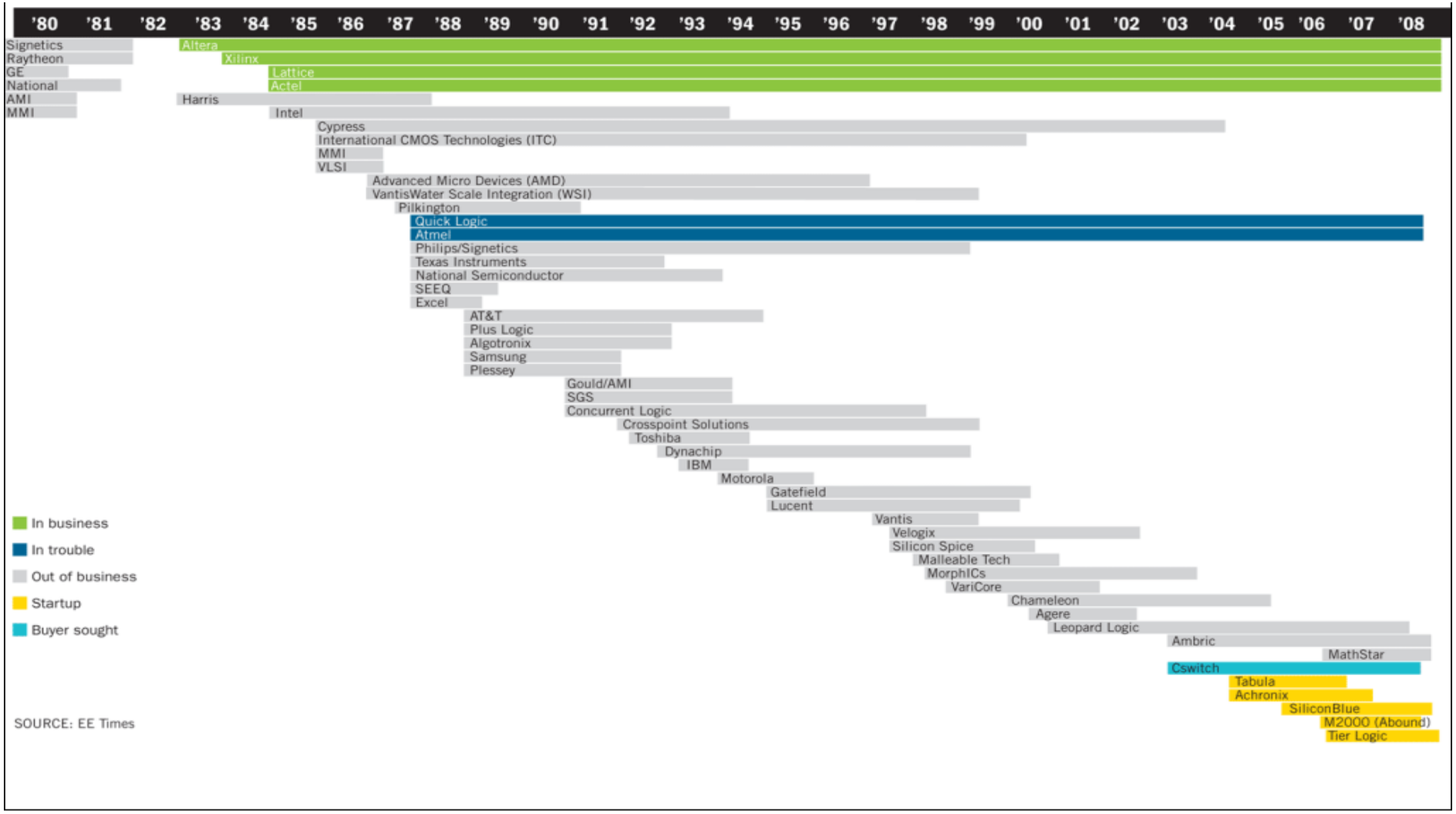


AMD
Atmel
Freescale
Infineon
Intel
Microchip
NXP
Renesas
Silicon Labs
Spansion
STMicro
TI
XMOS
:
etc.

ARM
CEVA
DCD
Imagination (MIPS)
:
etc.

Achronix
Altera
Atmel
Lattice
Microsemi
Tabula
Xilinx
:
etc.

ADICSYS
Menta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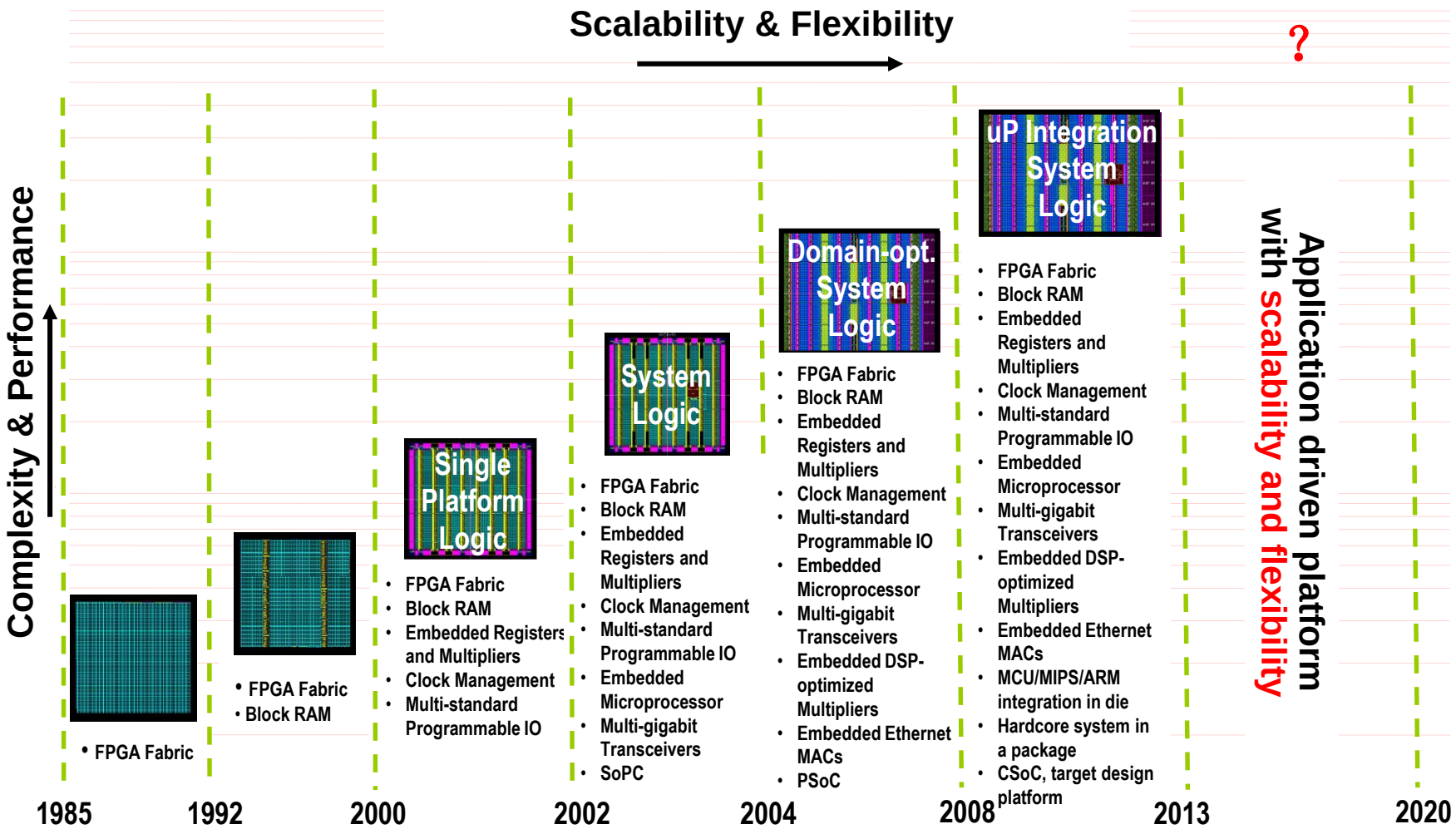
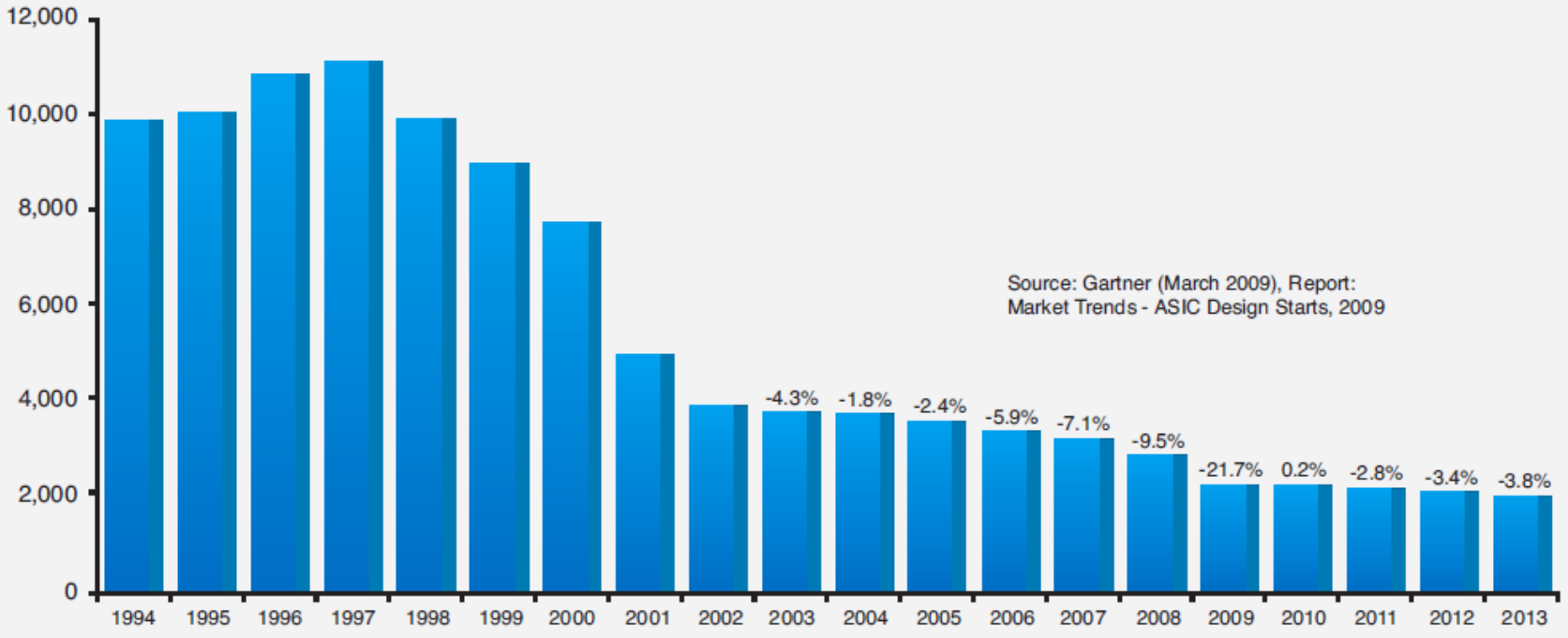
Signetics
Raytheon
GE
National
AMI
MMI
Altera
Xilinx
Lattice
Actel
Harris
Intel
Cypress
International CMOS Technologies (ITC)
MMI
VLSI
Advanced Micro Devices (AMD)
VantisWater Scale Integration (WSI)
Pilkington
Quick Logic
Atmel
Philips/Signetics
Texas Instruments
National Semiconductor
SEEQ
Excel
AT&T
Plus Logic
Algotronix
Samsung
Plessey
Gould/AMI
SGS
Concurrent Logic
Crosspoint Solutions
Toshiba
Dynachip
IBM
Motorola
Gatefield
Lucent
Vantis
Velogix
Silicon Spice
Malleable Tech
MorphICs
VariCore
Chameleon
Agere
Leopard Logic
Ambric
MathStar
Cswitch
Tabula
Achronix
SiliconBlue
M2000 (Abound)
Tier Logic
In business
In trouble
Out of business
Startup
Buyer sought
SOURCE: EE Times

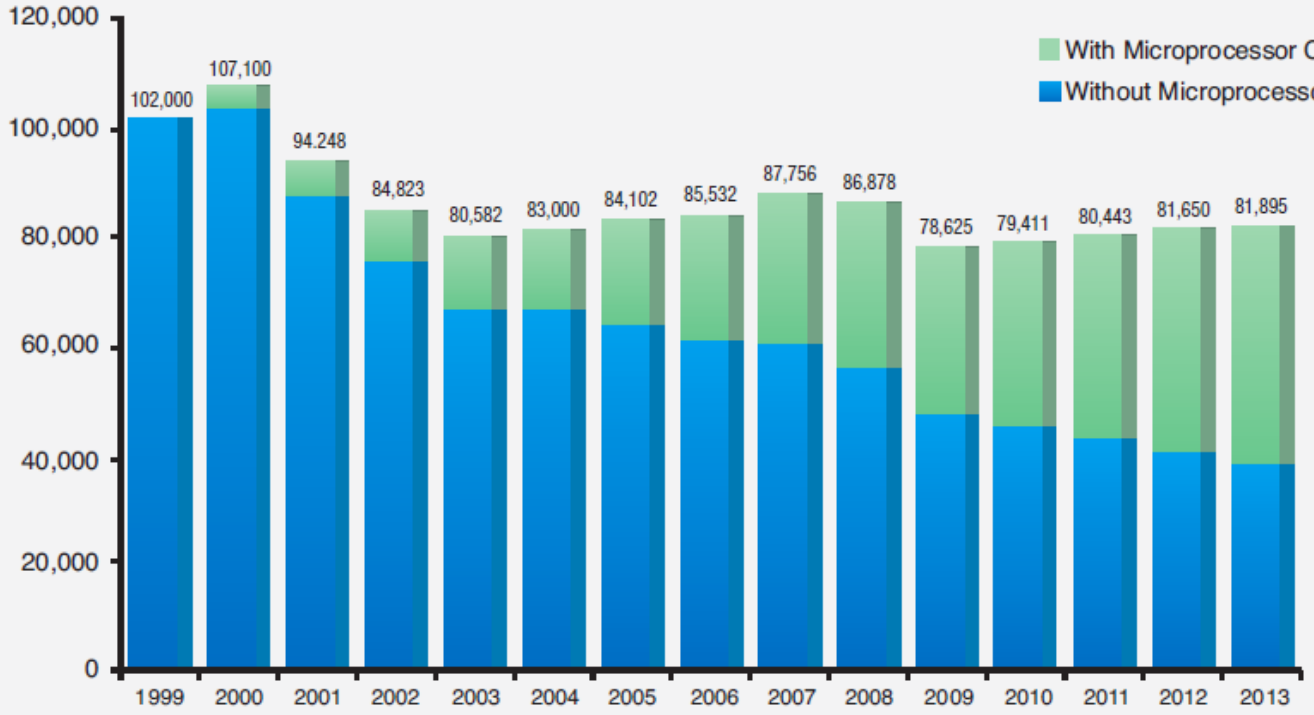

Scalability & Flexibility
Complexity & Performance
?
Application driven platform with scalability and flexibility
• FPGA Fabric
• FPGA Fabric
• Block RAM
Single Platform Logic
• FPGA Fabric
• Block RAM
• Embedded Registers and Multipliers
• Clock Management
• Multi-standard Programmable IO
System Logic
• FPGA Fabric
• Block RAM
• Embedded Registers and Multipliers
• Clock Management
• Multi-standard Programmable IO
• Embedded Microprocessor
• Multi-gigabit Transceivers
• SoPC
Domain-opt. System Logic
• FPGA Fabric
• Block RAM
• Embedded Registers and Multipliers
• Clock Management
• Multi-standard Programmable IO
• Embedded Microprocessor
• Multi-gigabit Transceivers
• Embedded DSP-optimized Multipliers
• Embedded Ethernet MACs
• PSoC
uP Integration System Logic
• FPGA Fabric
• Block RAM
• Embedded Registers and Multipliers
• Clock Management
• Multi-standard Programmable IO
• Embedded Microprocessor
• Multi-gigabit Transceivers
• Embedded DSP-optimized Multipliers
• Embedded Ethernet MACs
• MCU/MIPS/ARM integration in die
• Hardcore system in a package
• CSoC, target design platform
1985
1992
2000
2002
2004
2008
2013
2020

Estimated Worldwide ASIC Design Starts, 1994-2013 全球ASIC设计开始数量统计：1994-2013



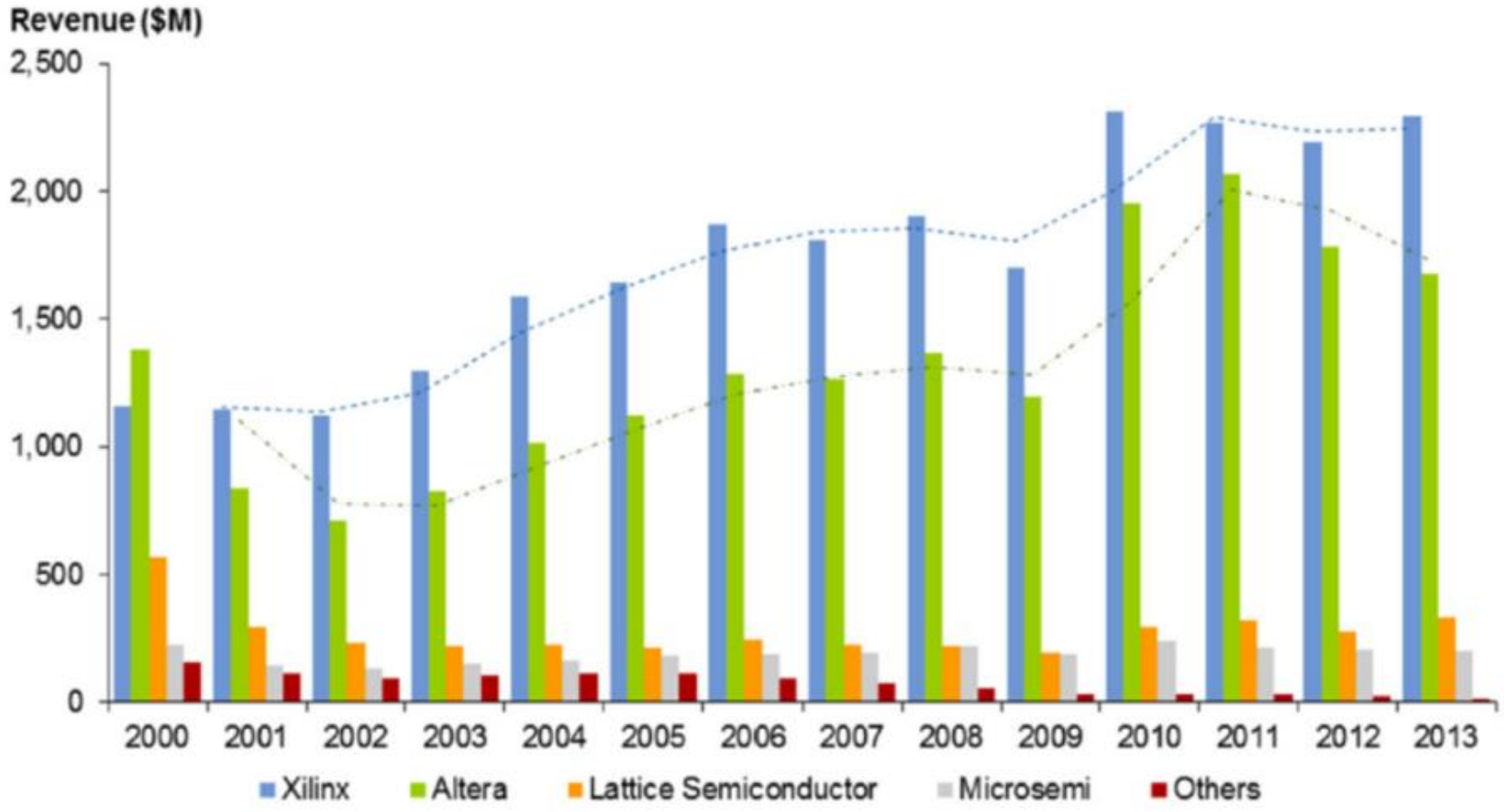
Estimated FPGA /PLD Design Starts, 2003-2013

全球FPGA/PLD设计开始数量统计：1999-2013



Source: Gartner (March 2009), Report: Market Trends - ASIC Design Starts, 2009

FPGA Vendors' Revenue, 2000 to 2013



FPGA = field-programmable gate array

Source: Gartner (October 2014)

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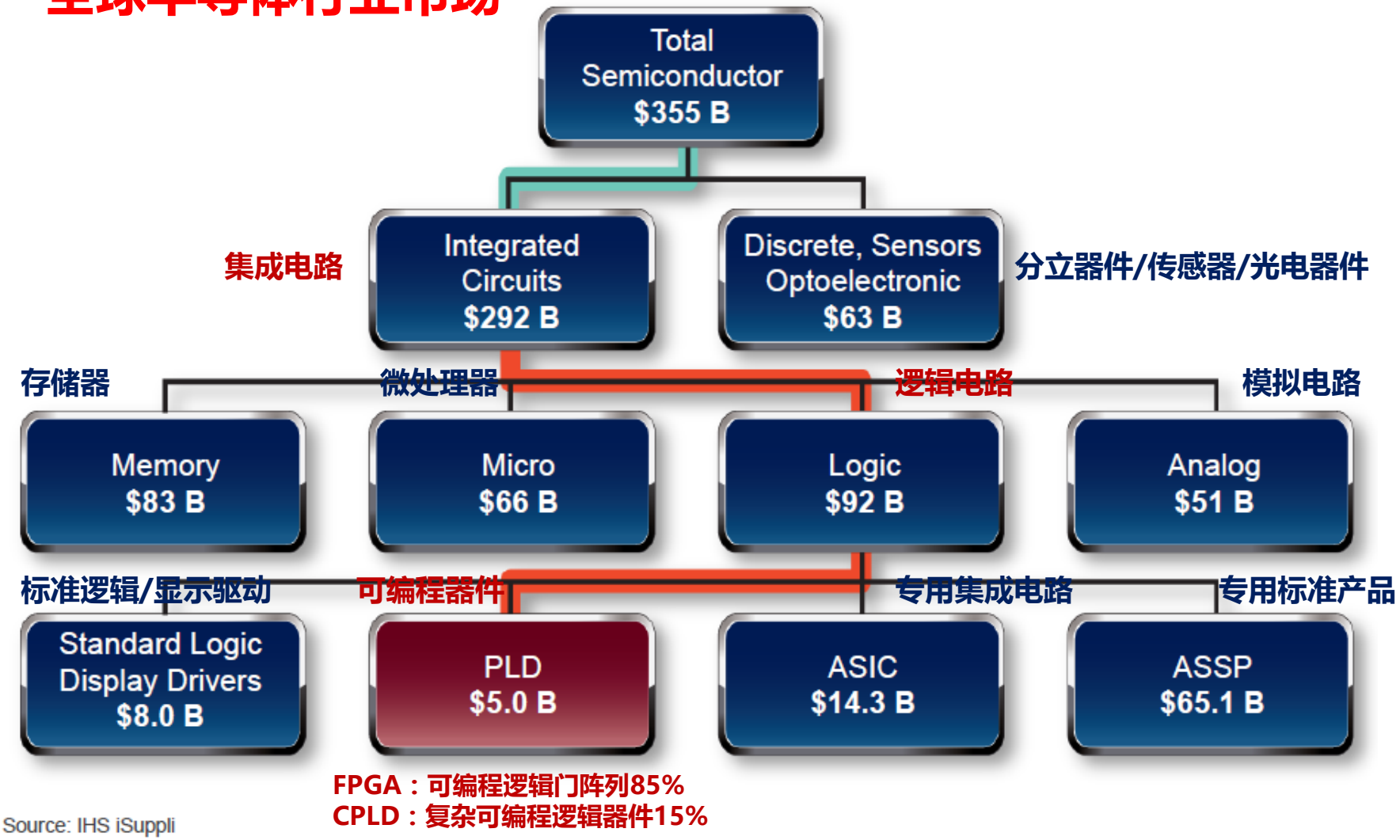
Worldwide Semiconductor Market - 2014

全球半导体行业市场



FPGA：可编程逻辑门阵列85%
CPLD：复杂可编程逻辑器件15%

Source: IHS iSuppli

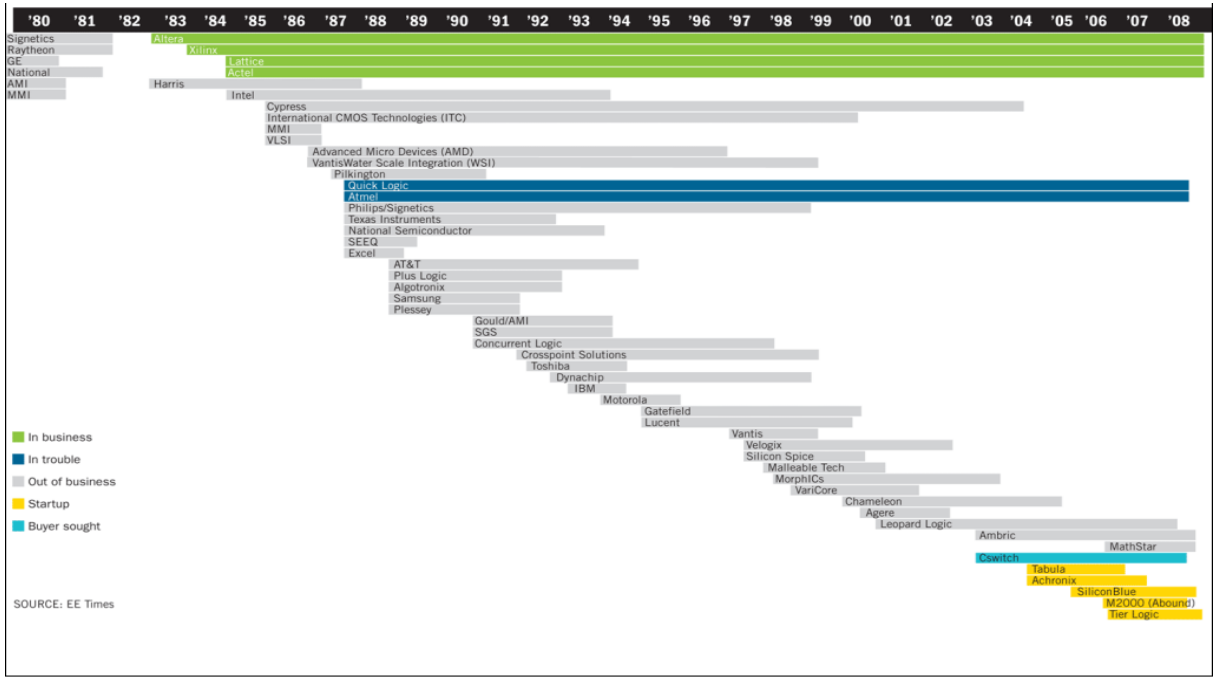
Key Attributes of FPGA, ASSP and ASIC Chips From the Equipment Perspective

Attributes	FPGA	ASSP	ASIC
Ability to Customize			
Fast Time-to-Market			
Mask/Yield/Design and Tool Costs			
Low Risk			
Suitable for Emerging Standards			
Suitable for High-Volume*			
Suitable for Highest Performance Designs			
Low Cost Per Chip			

Poor	Challenge	Average	Good	Excellent

Note: *There are cases when lower-end FPGA/PLDs can meet high-volume cost requirements.
ASIC = application-specific integrated circuit; ASSP = application-specific standard product; FPGA = field-programmable gate array; PLD = programmable logic device

Source: Gartner (October 2014)



Microsemi

2010.10
$430M

Actel

LATTICE SEMICONDUCTOR

2011.12
$63.2M

SiliconBlue

intel

2015.6
$16.7B

ALTERA MEASURABLE ADVANTAGE™

abound logic™

2010.6

menta

ADICSYS The Embedded FPGA Company

TIERLOGIC

2010.7

tabula

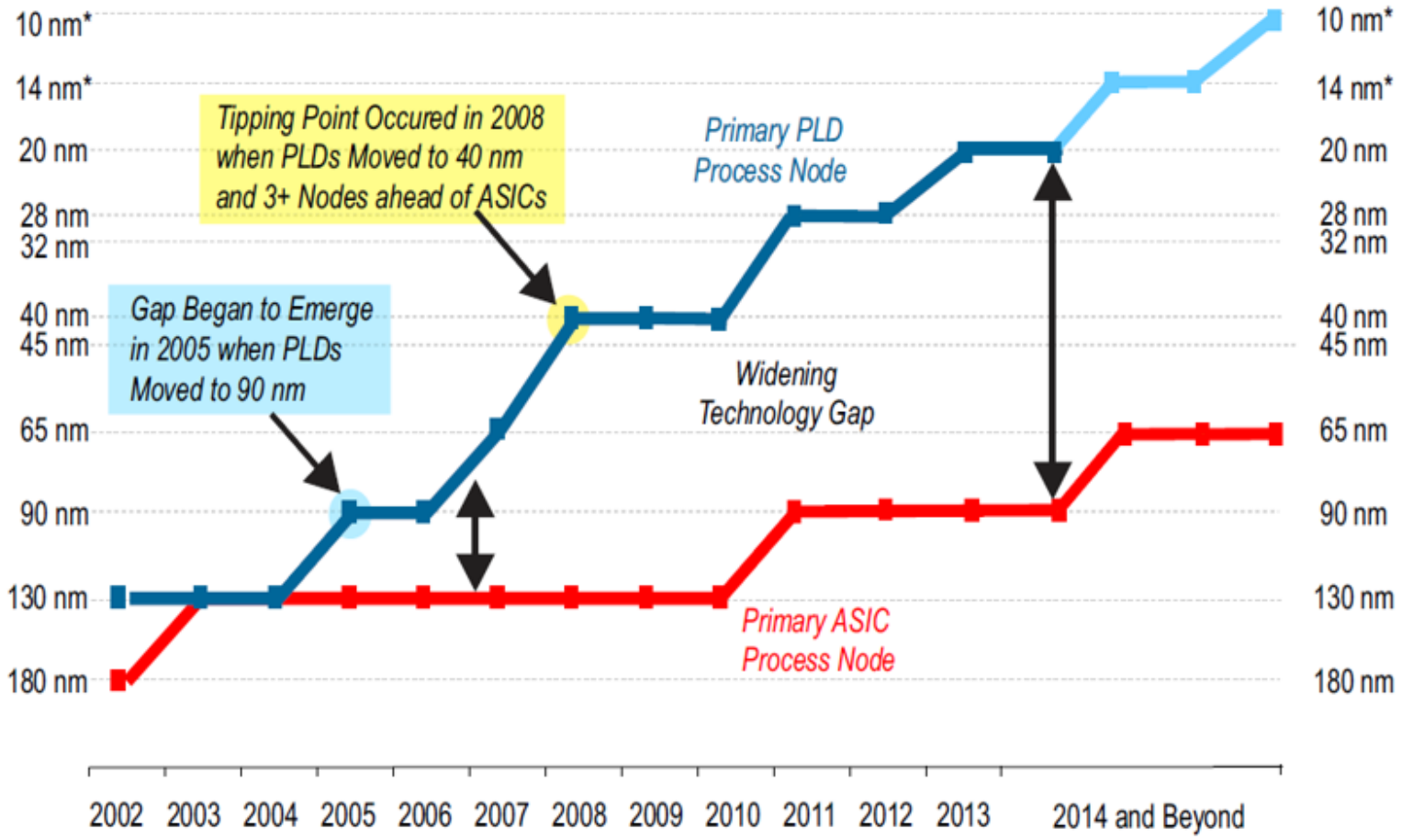
2015.1

EFINIX™

achronix SEMICONDUCTOR CORPORATION

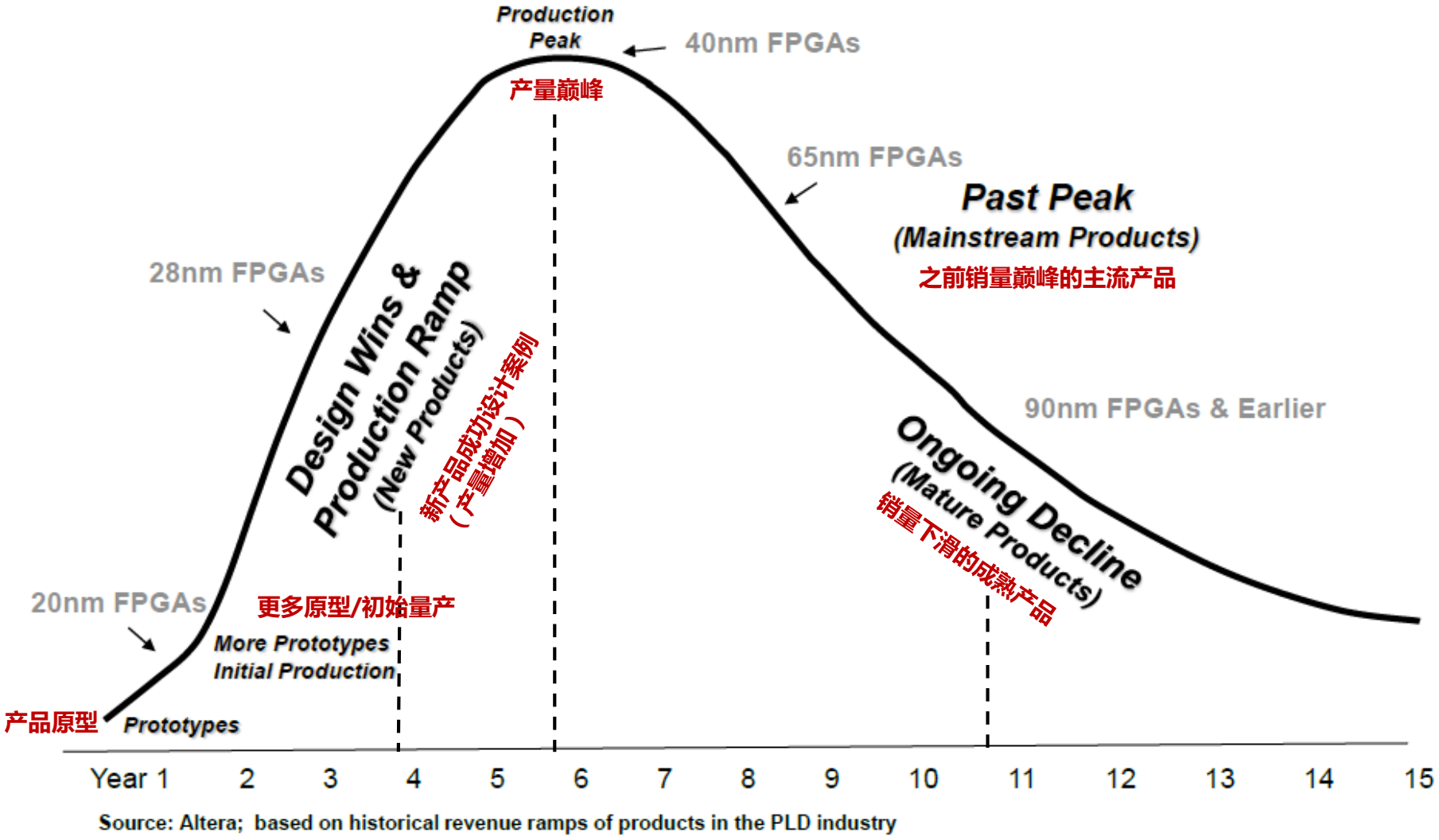
flexlogix Technologies, Inc.

Programmable Logic vs. ASIC Primary Process Nodes for New Designs



Source: Altera; Data applies to new design starts.

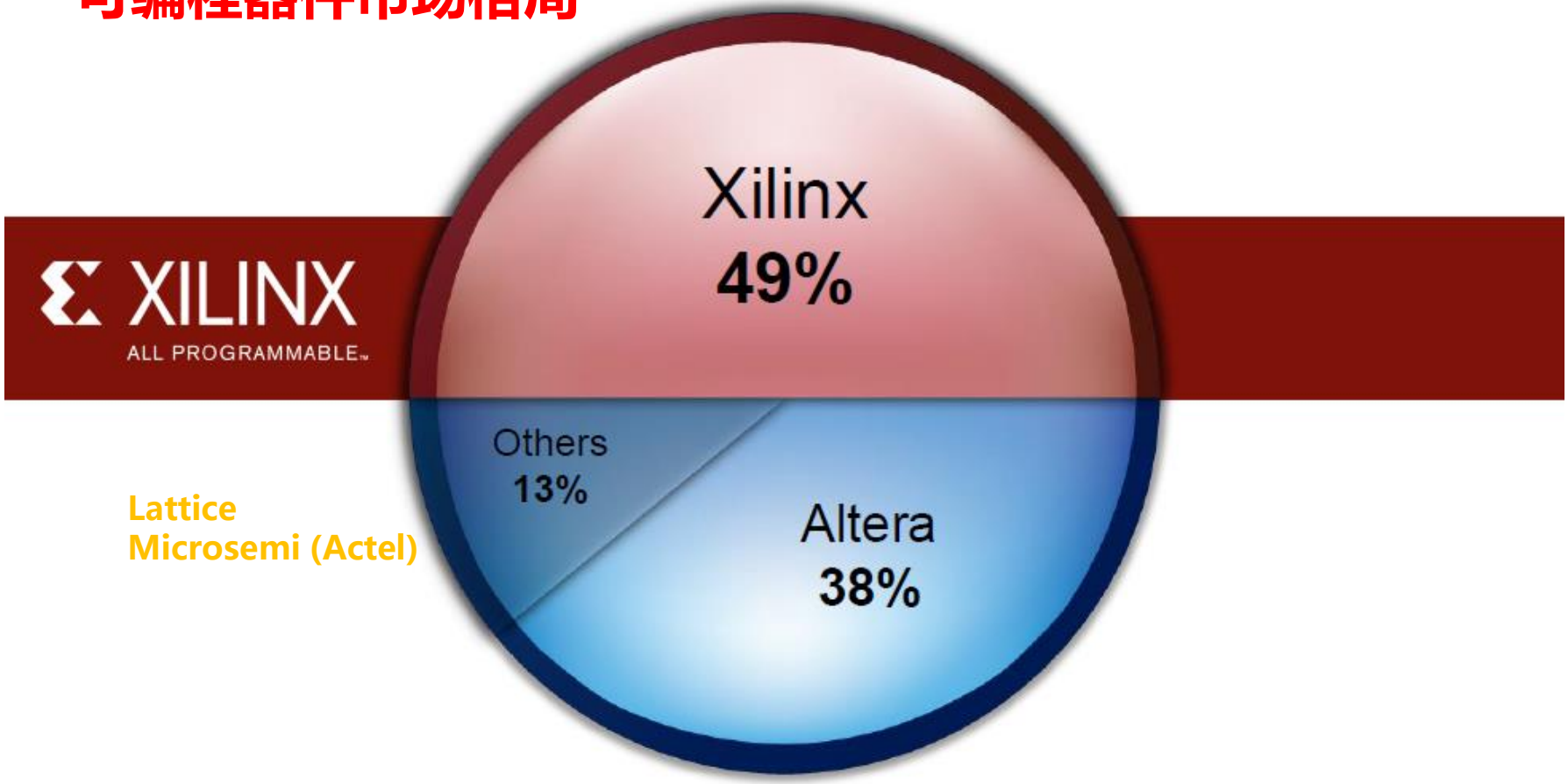
** FinFET Technology. Timeframe for PLDs on 14 nm and 10 nm FinFET technology to be announced.*



Source: Altera; based on historical revenue ramps of products in the PLD industry

PLD Market Share - Calendar Year 2014

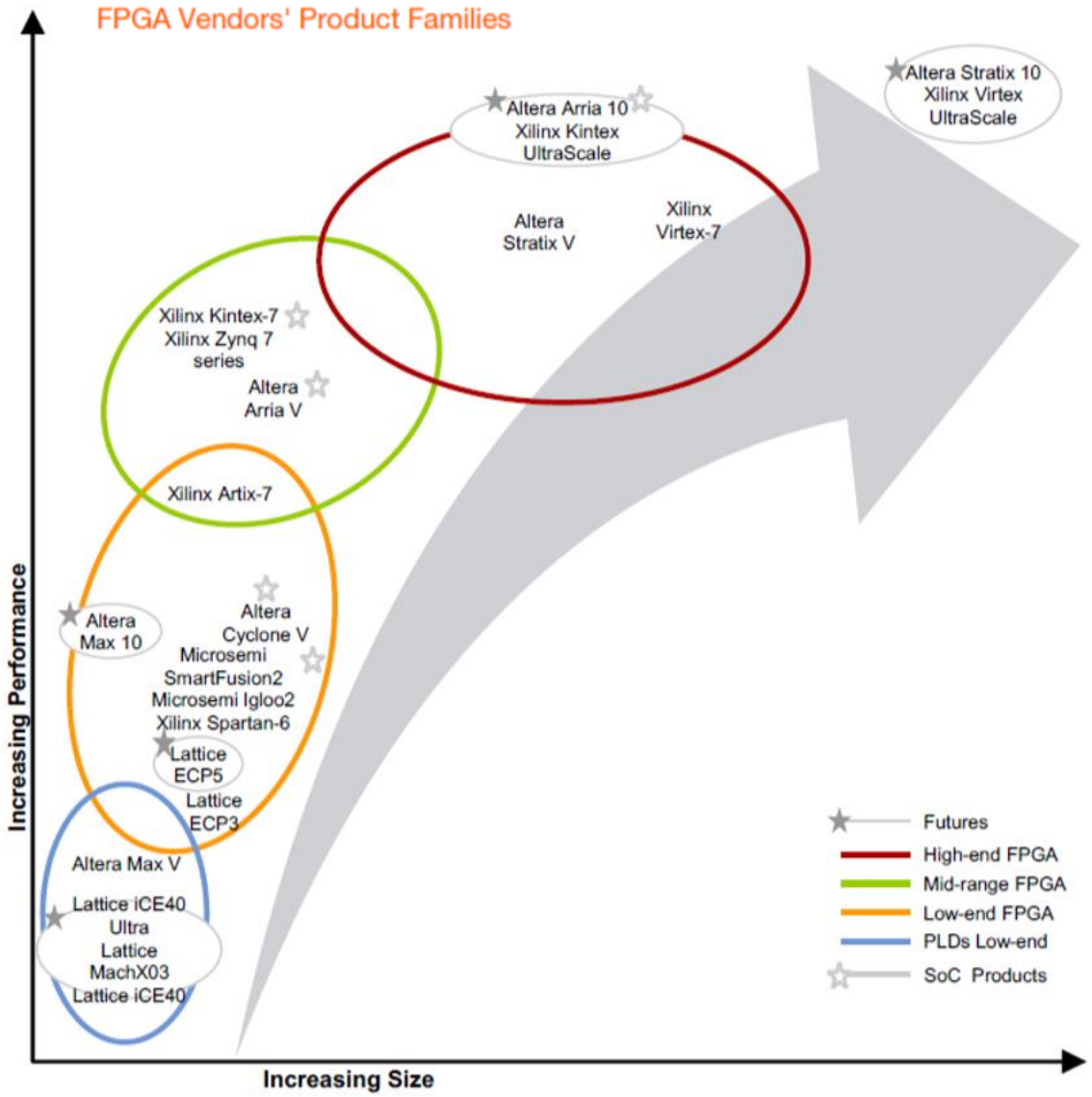
可编程器件市场格局



With nearly 50% Market Share, Xilinx is the #1 PLD Supplier

Xilinx仍然是世界上最大的可编程逻辑器件供应商，2014年市场占有率将近50%

Source: IHS iSuppli



FPGA = field-programmable gate array; PLD = programmable logic device; SoC = system-on-chip

Source: Gartner (October 2014)

Segments of the Programmable Market

Segment	Characteristics	Applications	Vendor Offerings
High-end FPGA category (ranges from 200K to 2,000K LCs).	Performance and size are the most important considerations. These devices favor high-complexity, lower volume and larger designs that are not power- or cost-sensitive.	At this end of the market, providers favor use cases and applications in which customization is important — but for which ASICs are either too expensive, risky or time-consuming to be used effectively. Key applications are in the wired communications, industrial and military sectors.	Xilinx and Altera are both pushing the latest node. Both companies compete directly with their Virtex and Stratix products, respectively.
Midrange FPGA category (ranges from 25K to 505K LCs).	The midrange of the market focuses on designs that are slightly smaller and lower-cost, but where good to excellent performance is still required.	Examples of applications in this segment include base stations, surveillance systems and solid-state drives.	Most competition in this space is between Altera and Xilinx. New devices that have been announced and which are in early-phase production include Altera's Arria 10 and Xilinx's Kintex UltraScale.
Low-end FPGA category (2K to 301K LCs).	The low end of the FPGA market typically suits requirements for larger "glue logic," and sometimes incorporates higher-level blocks of logic.	Applications in aerospace and military systems with strong environmental requirements; and in communications and industrial systems where reliability, security and persistence are desirable.	All four vendors (namely Altera, Lattice Semiconductor, Microsemi and Xilinx) have offerings in this category. Microsemi's non-volatile, mostly Flash-based offerings favor most applications.
PLD category (up to 30K macrocells or LCs).	Dominated by lower-power, lower-cost and higher-volume applications, or "glue logic."	Particularly suited to cost-sensitive and low-power applications that require interface and bridging, sensor fusion, basic "glue logic" and other companion chip functionality. They are also usable in many low-power IoT applications.	All four vendors compete here, although Lattice Semiconductor has carved out a niche for itself at the very low end with its iCE family of parts. These are designed into several Samsung Electronics smartphones. Microsemi targets military applications such as drones and surveillance systems.

ASIC = application-specific integrated circuit; FPGA = field-programmable gate array; IoT = Internet of Things; K = thousands; LC = logic cell; PLD = programmable logic device

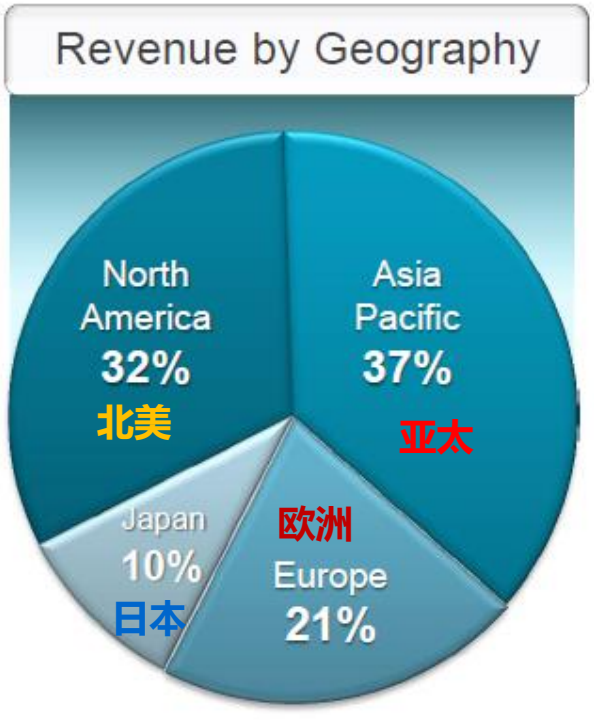
Source: Gartner (October 2014)

Revenue Breakdown - March Quarter 2015

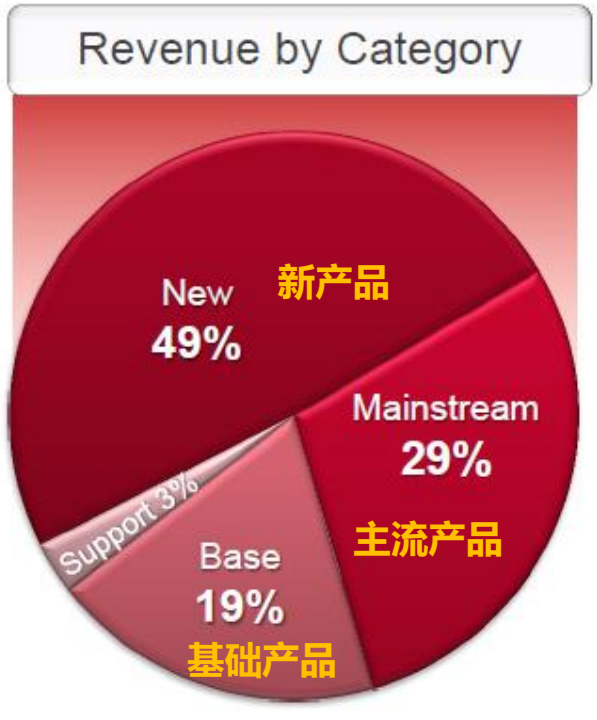
Xilinx收入分解 - 2015年第一季度

XILINX
ALL PROGRAMMABLE.

按终端市场分类



按地域分类



按产品分类

Serving a Wide Range of Markets

Xilinx产品服务广泛的市场

XILINX
ALL PROGRAMMABLE

Aerospace and Defense
- Avionics, MILCOM
- Space

航空航天与国防

Communications
- Wired and wireless networking
- Data center

通信

Industrial, Scientific, Medical
- Ultrasound systems
- Motor controllers

工控/科学/医疗

Audio, Video, Broadcast
- 3D cameras
- Video transport

声音/视频/广播

Automotive
- Infotainment
- Driver assistance

汽车电子

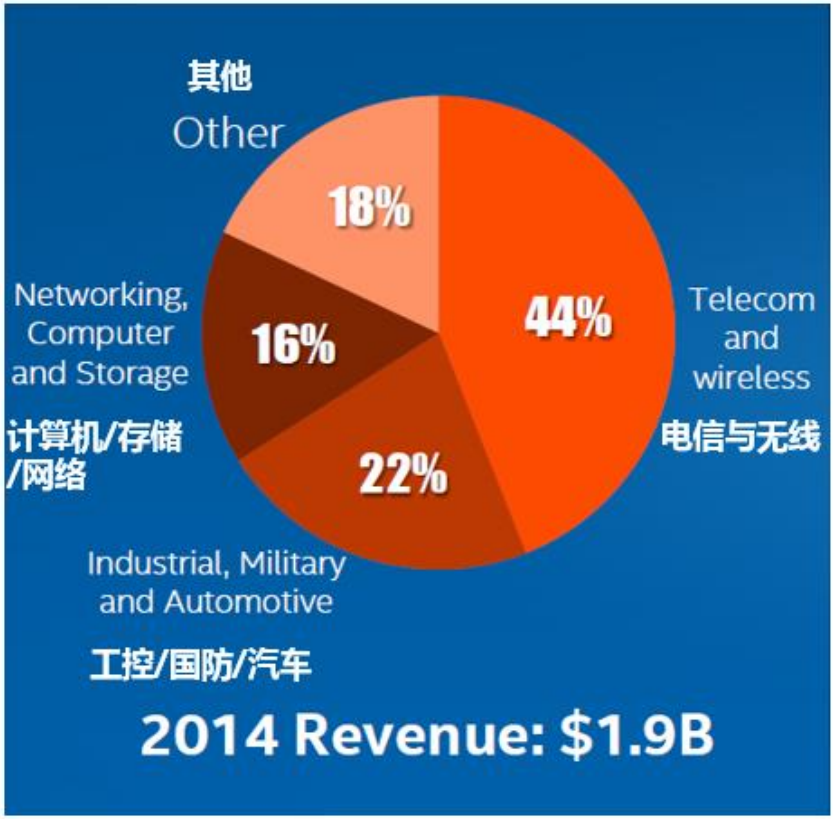
Consumer
- Multi-function printers
- eReaders

消费电子

Test & Measurement
- Communications instruments
- Semiconductor ATE

测试与仪器

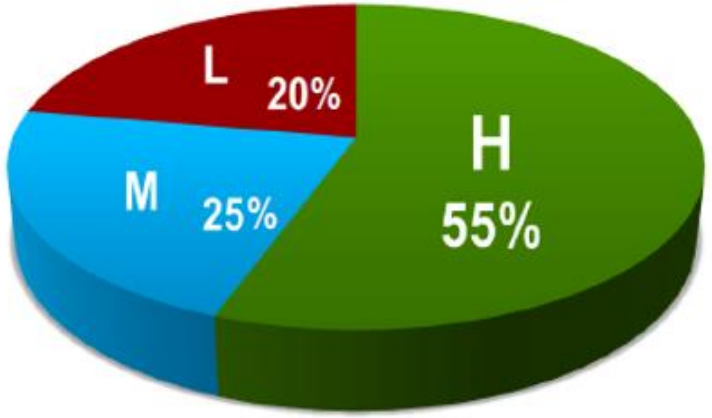
Sizing the Markets, Sizing the Products



Total FPGA Revenue By FPGA Class
Projected for 28nm, 20nm, 14nm

H = High end M = Mid-range L = Low end

H高端；M中端；L低端



ALTERA
MEASURABLE ADVANTAGE™

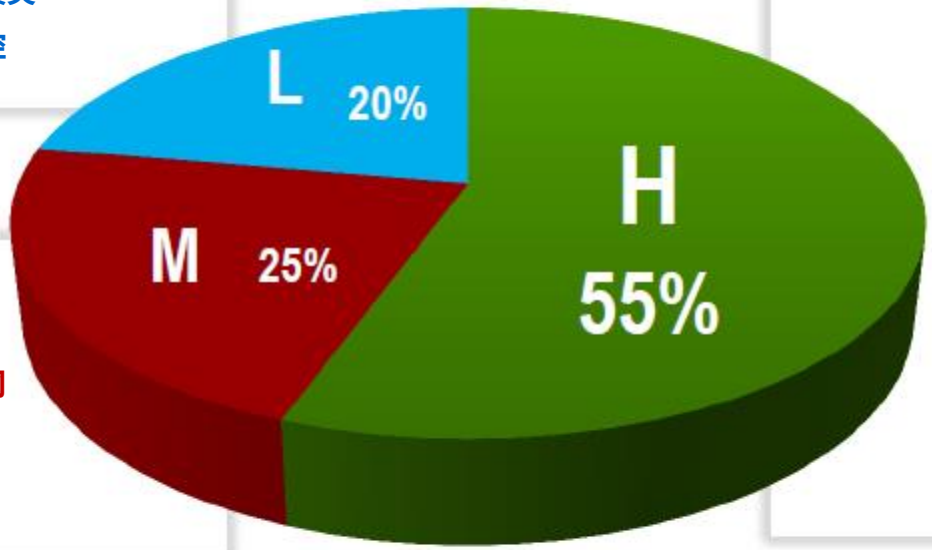
Diverse markets served by a portfolio of FPGAs

The Displacement Opportunity
Altera产品取代其他产品的机会

- Automotive 汽车电子
- Consumer 消费类
- Industrial 工控

- Broadcast 广播
- Networking (enterprise) 网络 企业网
- Wireless (radio) 无线 电台

H高端；M中端；L低端



- Computer & Storage 计算机/存储
- Medical 医疗
- Military 国防
- Networking (service provider) 网络
- Telecom 电信
- Test & Measurement 测试/仪器
- Wireless (baseband & radio) 无线

被取代的产品种类

ASSP ASIC DSP MCU CPU GPU

Products to be displaced

ALTERA MEASURABLE ADVANTAGE™

COMPELLING MARKET OPPORTUNITIES

Increasing Complexity & Connectivity

LATTICE SEMICONDUCTOR

Lattice产品为创新应用提供机会

GROWING APPLICATIONS

消费

CONSUMER

Internet of Things (IoT), Smartphones, Tablets, Wearables, Smart TV

物联网/智能手机/平板/可穿戴/智能电视

工控

INDUSTRIAL

Surveillance, Human-Machine Interface (HMI), Automation

智能监控/人机接口/自动化

通信

COMMUNICATIONS

Small Cells, Backhaul, Wired Access, Aggregation

小基站/传输网络/有线接入/汇聚网

DRIVERS & NEEDS

Mobile Revolution

- Connecting everything
- Rapidly decreasing price points
- Low power

无缝连接/成本敏感/低功耗

Industrial Evolution

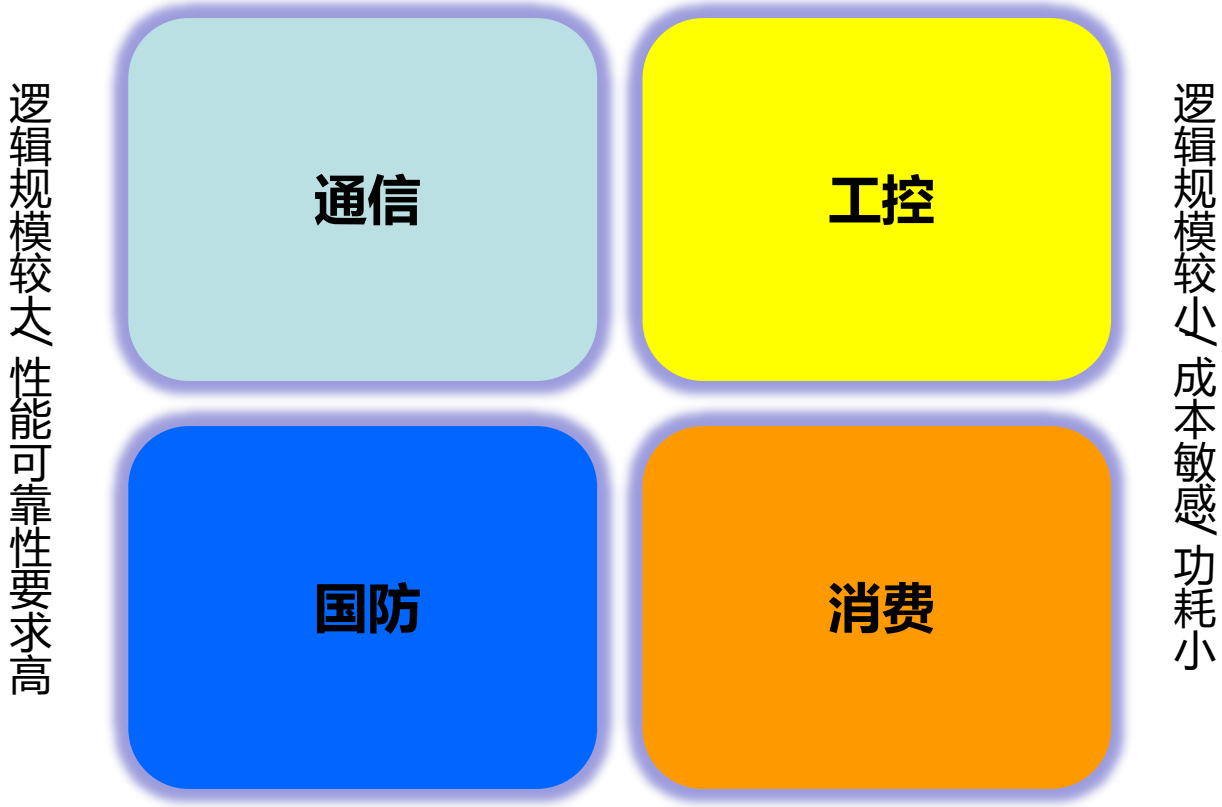
- Sensor proliferation
- Improved machine vision analytics
- Virtual reality

集成传感器/提高机器视觉分析/虚拟现实

Infrastructure Loading

- Mobile data traffic increase
- Rapid transition to cloud-based infrastructure

移动数据业务增长/转移到云计算架构



四大主战场

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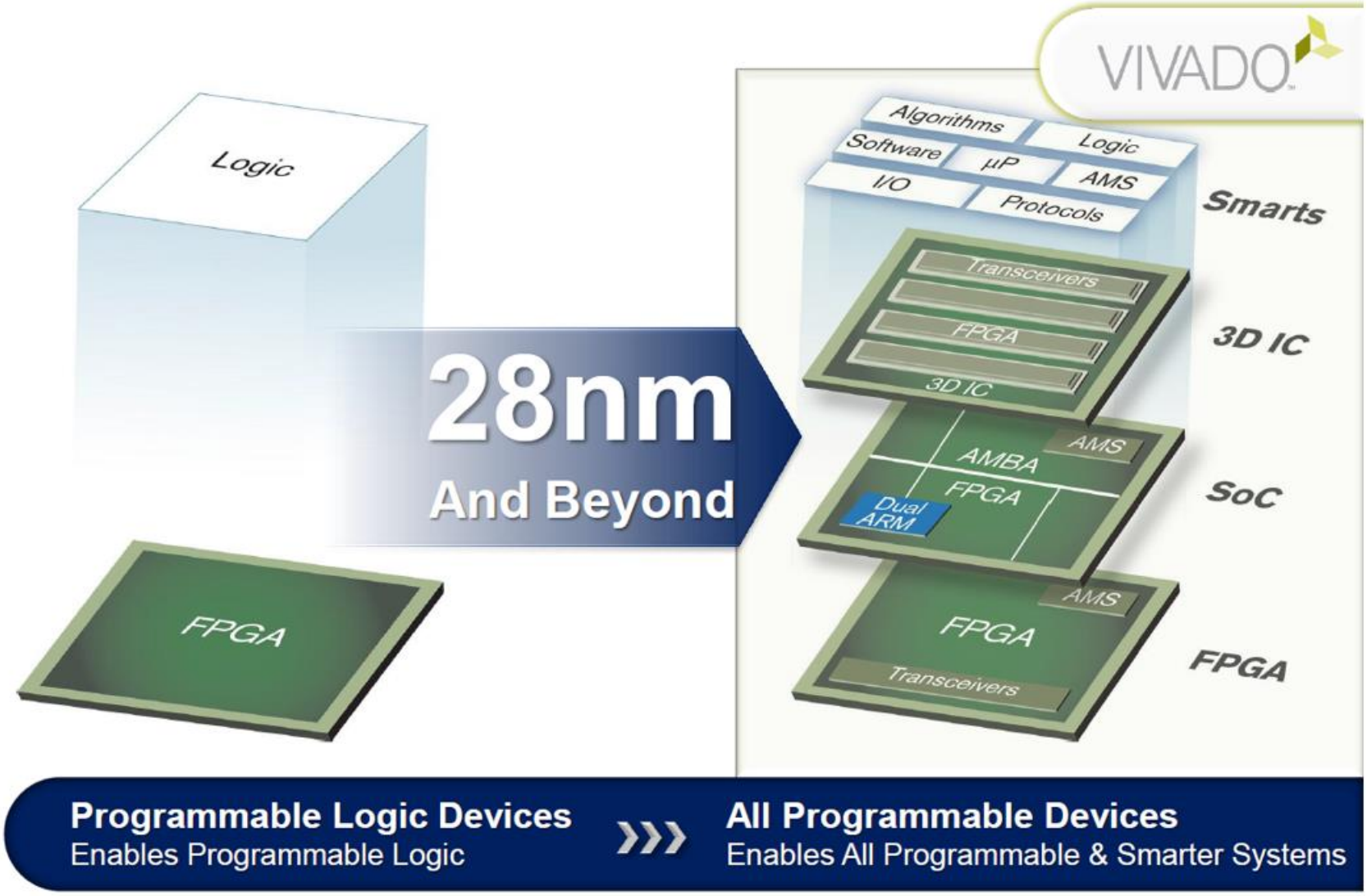
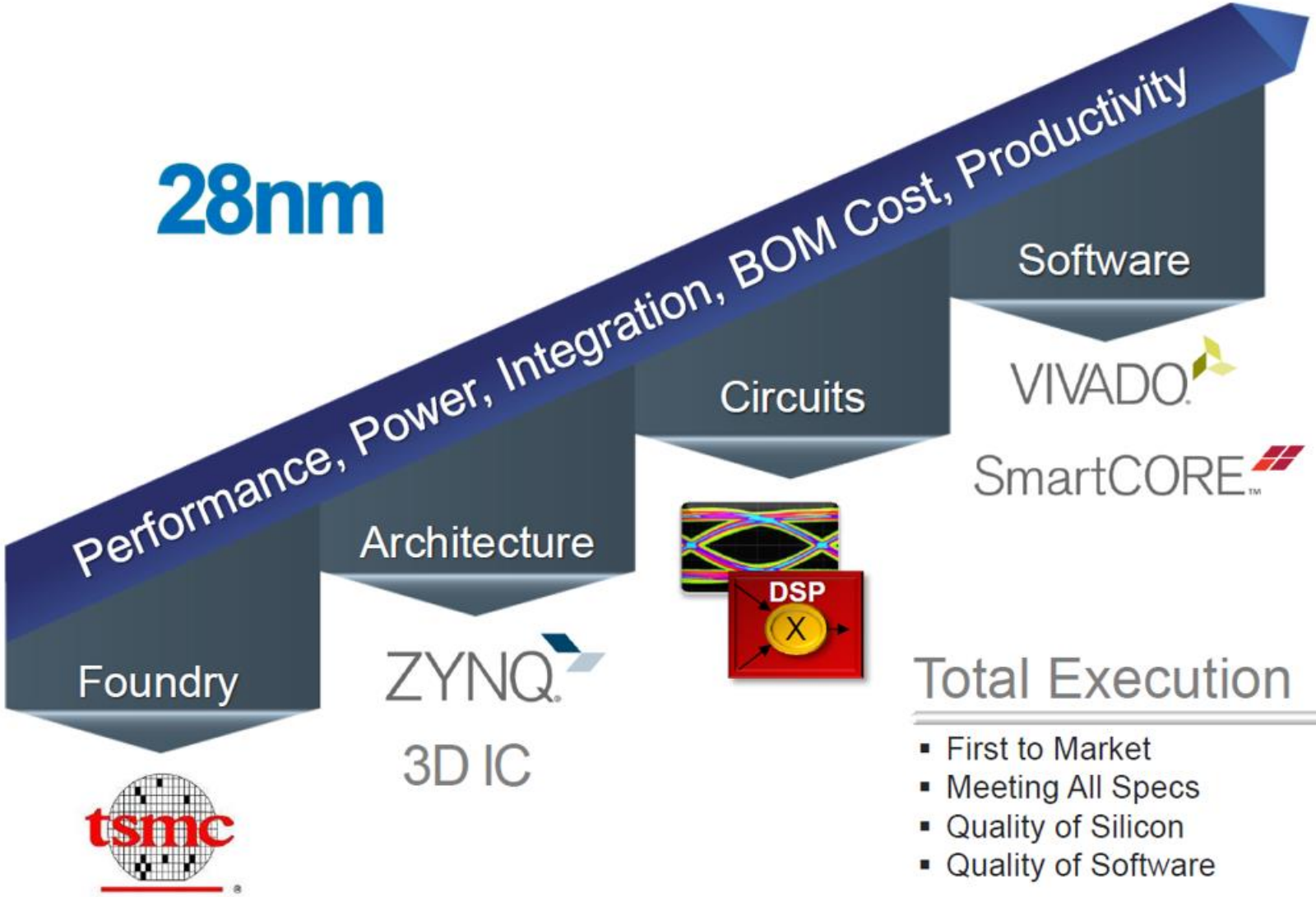
- 思考现在
- 展望未来

Delivering A Generation Ahead



XILINX ALL PROGRAMMABLE.

Proven Formula: 5 Strategic Advantages at 28nm

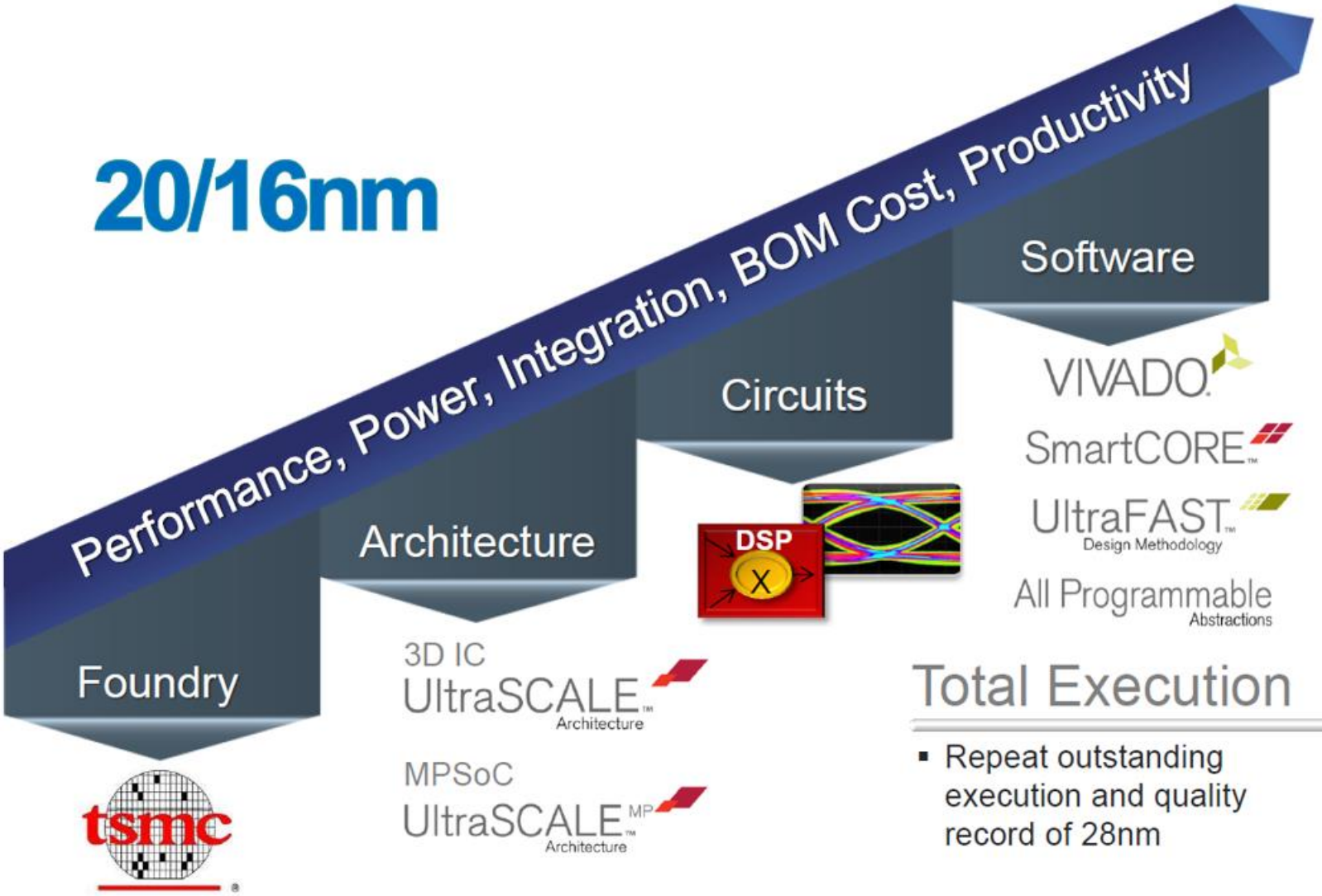


Total Execution

- First to Market
- Meeting All Specs
- Quality of Silicon
- Quality of Software

XILINX ALL PROGRAMMABLE.

Proven Formula: 5 Advantages for 20/16nm



Total Execution

- Repeat outstanding execution and quality record of 28nm

XILINX ALL PROGRAMMABLE

Proven Formula for Share Gains

XILINX ALL PROGRAMMABLE.

Focus on Industry Growth Megatrends

Smarter Data Centers

Smarter Vision & Connected Control

Programmable Imperative

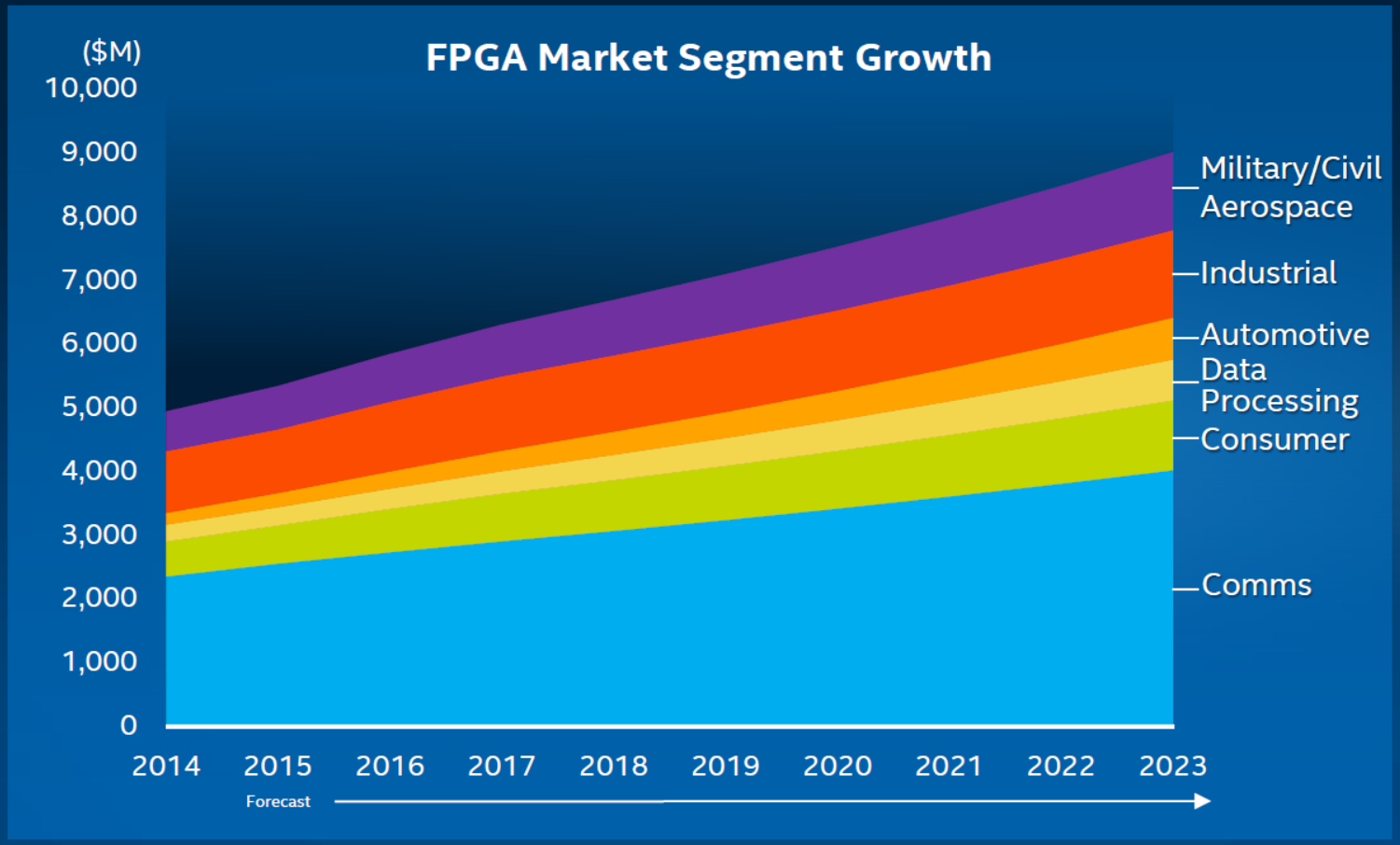
Smarter Nx100G Wired Networks

More Growth Markets

Smarter Wireless HetNets

XILINX ALL PROGRAMMABLE.

...In a Growing Market Segment



CAGR 7%

Source: Gartner

Cloud Example: Data Center FPGA Acceleration

Up to 1/3 of Cloud Service Provider Nodes to Use FPGAs by 2020

	Image Identification	Security	Big Data
Applications:			
			
Algorithms:	Convolutional Neural Network	Encryption	Compression

CPU	FPGA	CPU	FPGA	CPU + FPGA
Discrete FPGA		Co-Packaged CPU + FPGA		Integrated CPU + FPGA

Today →

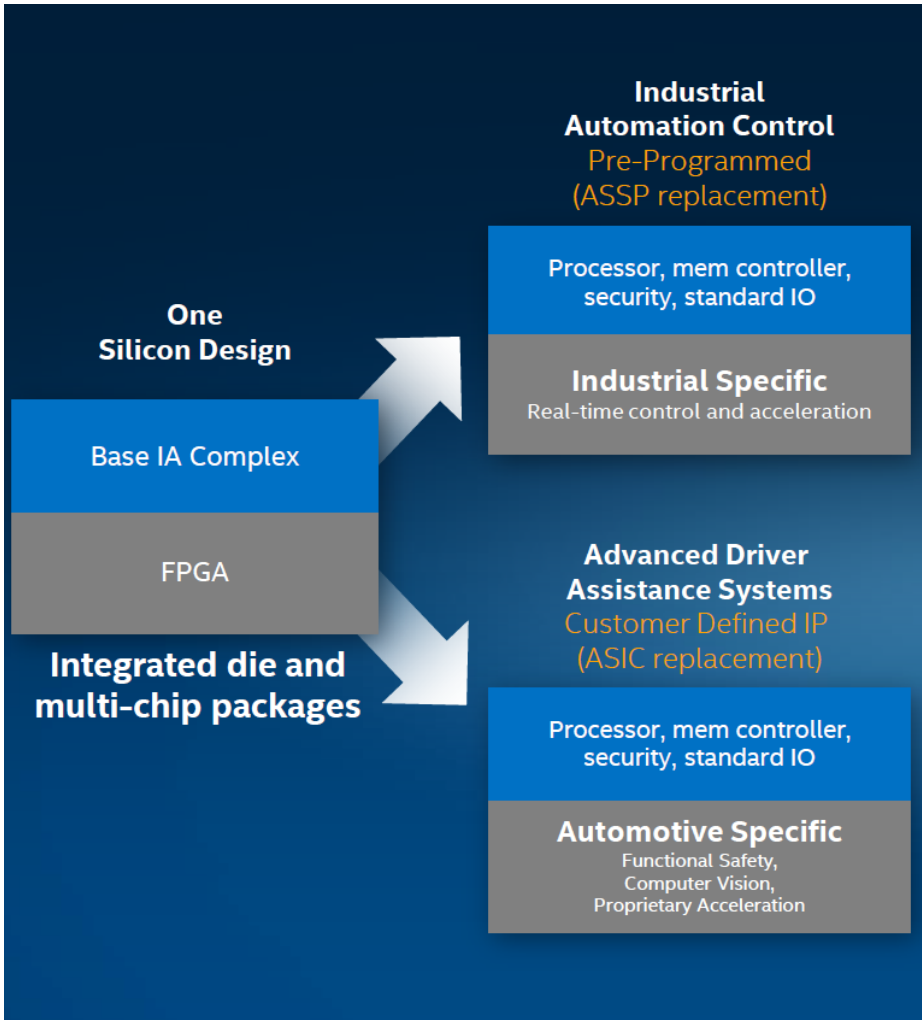
>2X performance increase through integration

Reduces total cost of ownership (TCO) by using standard server infrastructure

Increases flexibility by allowing for rapid implementation of customer IP and algorithms

https://gigaom.com/2015/02/23/microsoft-is-building-fast-low-power-neural-networks-with-fpgas/

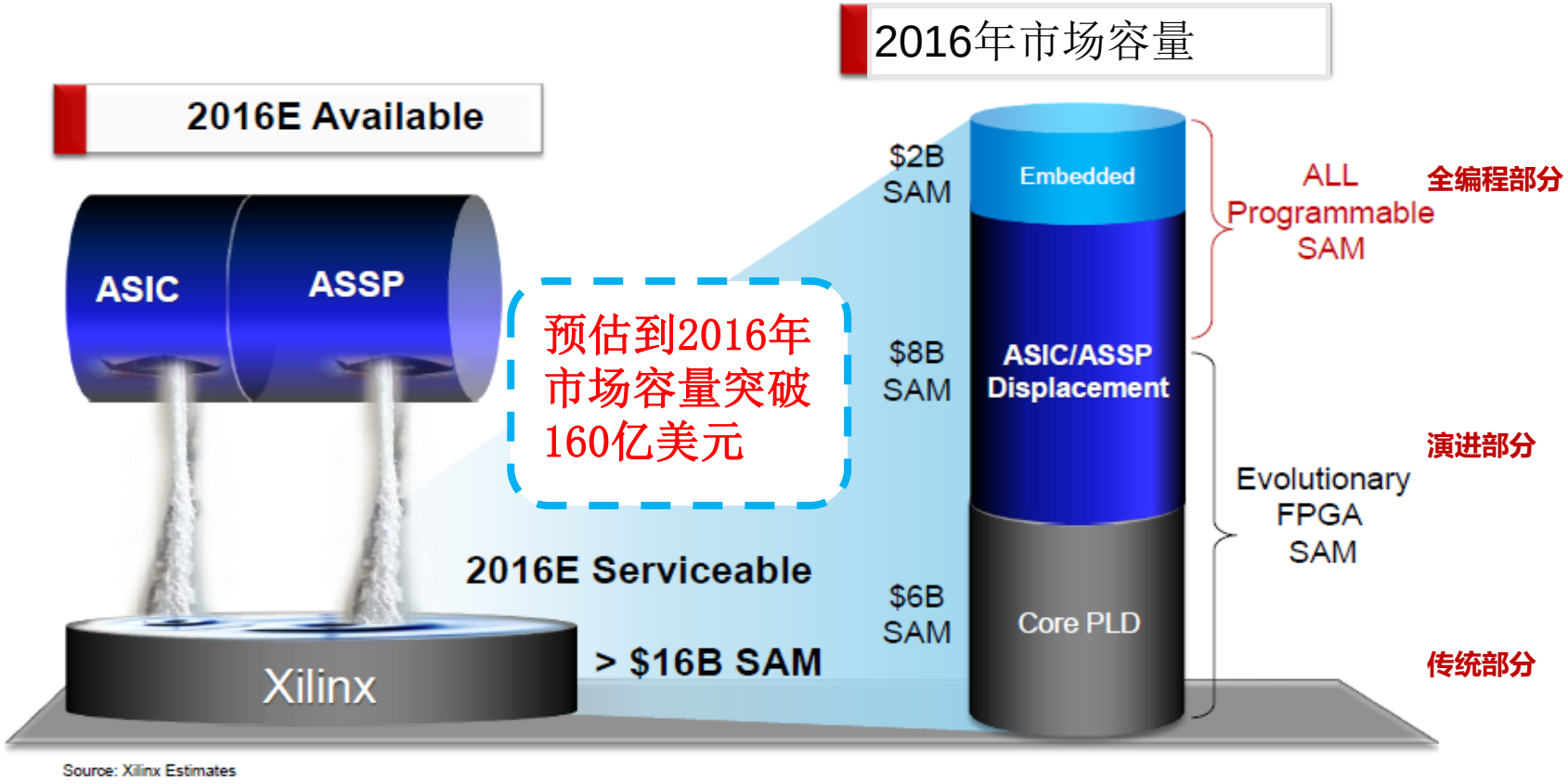
IoT Application Examples



- **Integrated solutions accelerate growth in key IoT segments by adding new functionality, improving performance, and lowering cost**
- **~$11B incremental SAM by 2020 as integrated FPGAs become cost competitive with ASICs & ASSPs**
- **Customers can program their own IP, replacing ASICs**
- **Intel can pre-program industry-specific IP, replacing ASSPs**
- **Expected to reduce time-to-market by more than 50%**

预计2022至2032年所有SOC系统芯片将全部具有可编程功能

Y14: 5B -> Y16: 16B
年复增长率CAGR: ~79%



附录：中国FPGA厂商何去何从？

京微雅格
Capital Microelectronics

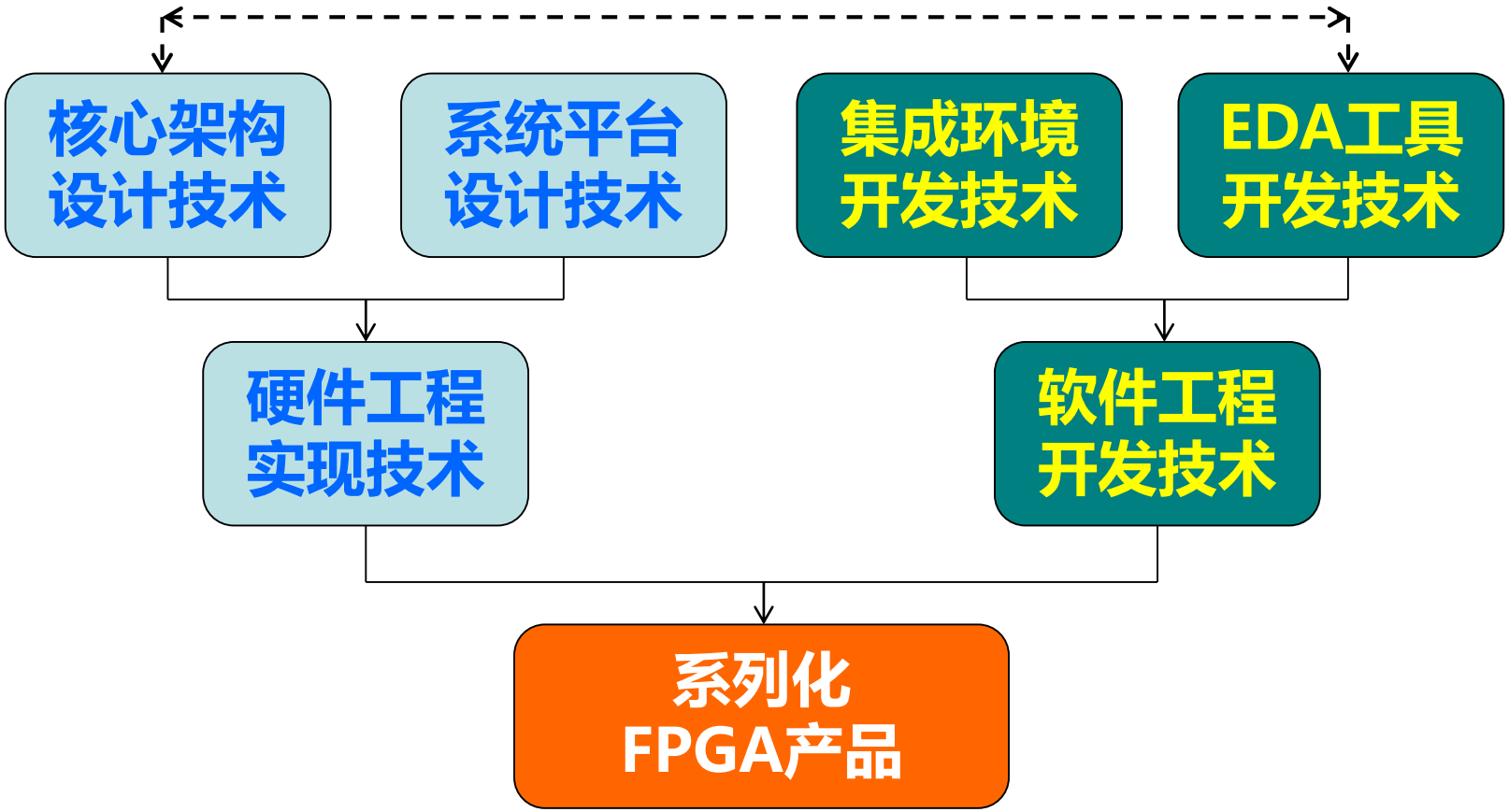
深圳市同创国芯电子有限公司
SHENZHEN PANGO MICROSYSTEMS CO.,LTD

FM
复旦微电子集团

GOWIN高云

安路科技
ANLOGIC

需要有系列化的FPGA产品



X/A/L公司的专利技术中50%以上是保护核心架构的专利！

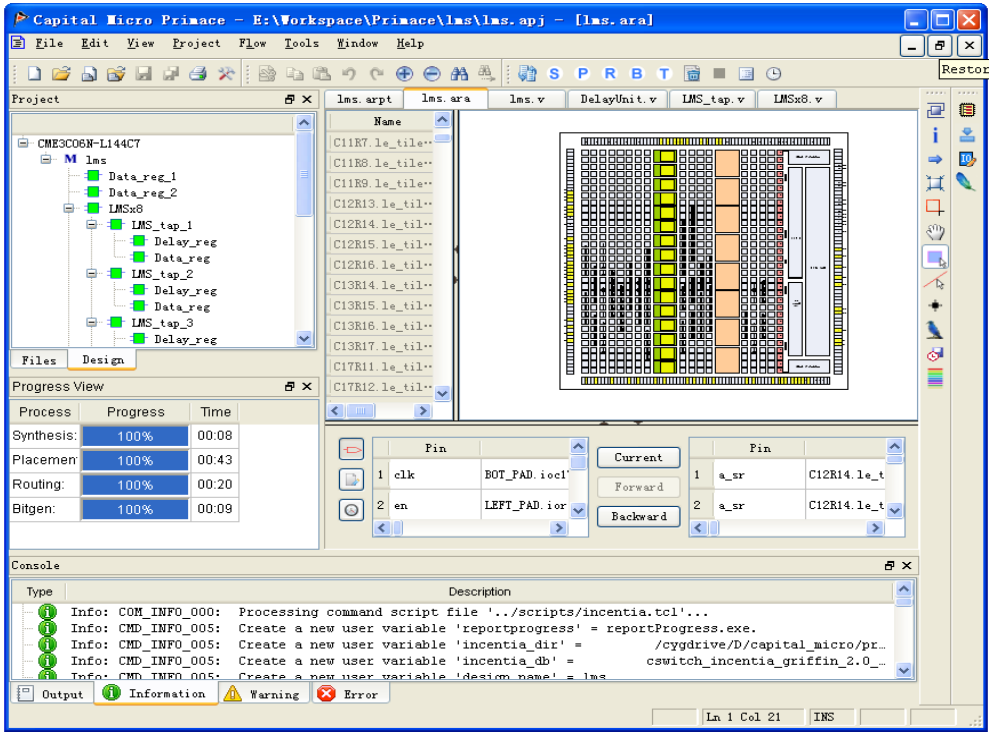
自主知识产权的FPGA产品，首先体现在具备自主研发可编程逻辑器件**核心架构**的能力！

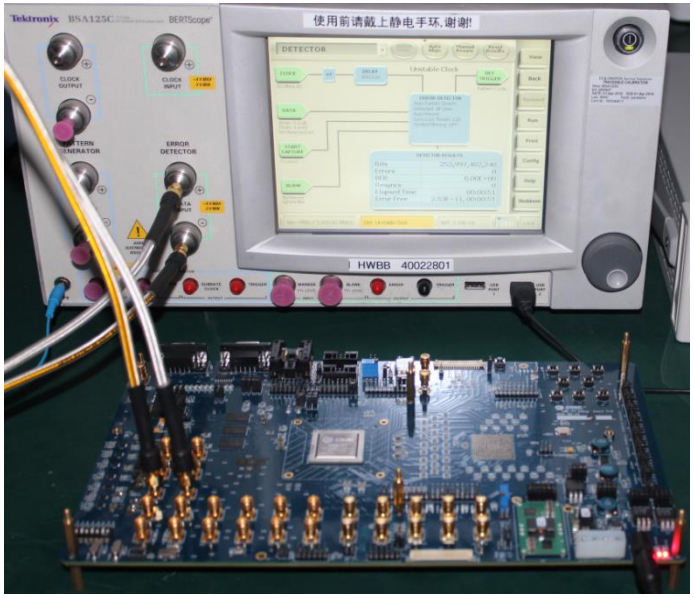
自主知识产权的FPGA产品，其次体现在具备自主研发FPGA器件配套软件工具的能力！

- 用户易用性、友好性、面向应用的软IP库支持、以及EDA工具性能和成熟度方面

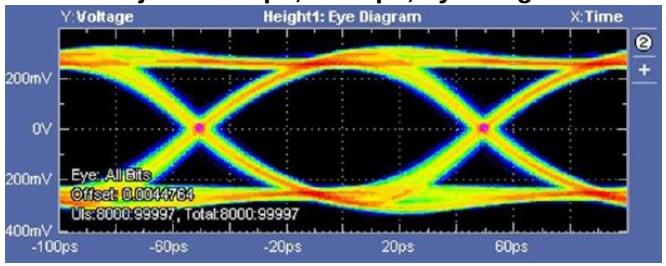
高端FPGA器件要想产业化，软件工具的好坏是决定性的因素！

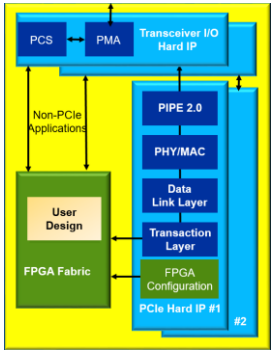
CME-C1千万门级中高端国产FPGA问世





Total jitter=24.6ps, 10Gbps, Eye Diagram





CME-C1芯片对标

	Altera	Xilinx	Lattice	Microsemi	CME
Part Number	EP4SGX70	XC6VLX75T	ECP5-45	M2S050	C1
Process	40nm TSMC	40nm UMC	40nm Fujitsu	65nm UMC	40nm TSMC
LUT Architecture	8 input LUT	6 input LUT	4 input LUT	4 input LUT	6 input LUT
Equivalent LUT4	73K	74.5K	44K	48.6K	57.6K
LUT6	N/A	46k	N/A	N/A	36K
REG	58K	93K	44K	48.6K	74K
LRAM	908Kbit	1045Kbit	351Kbit	N/A	576Kbit
EMB	6.4Mbit	5.6Mbit	1.944Mbit	1.826Mb	2.53Mbit
DSP (18x18)	384	288	72	72	288
PLL	4	6	4	6	4
IO	480	360	245	377	477
SerDes	16 (8.5Gbps)	12 (6.6Gbps)	4 (3.2Gbps)	8(5Gbps)	4 (10Gbps)
PCIe Gen2.0	YES	YES	NO	Yes	Yes
DDR3	1067Mbps	N/A	800Mbps	667Mbps	1333Mbps
LVDS Pair (Inputs/Outputs)	1.6Gbps (128)	1.3Gbps	800Mbps	700Mbps	1.3Gbps (144/144)
ADC	N/A	N/A	N/A	N/A	Dual 12 bit
Status	Production	Production	Production	Production	Production

路漫漫其修远兮 吾将上下而求索

京微雅格
Capital Microelectronics

谢谢！

hlwang@capital-micro.com